Important Notice

Atmel AT89S Microcontroller Family - In-System Programming Problems
Programmers affected: Equinox Micro-ISP Series III/IV, Activ8r (8051)
Version: 1.00, last updated 28/6/99

Warning
The Atmel AT89S Microcontroller Family has a problem which can stop a device being re-programmed more than once in 'In-System Programming' mode. This problem is caused by a silicon bug and is therefore beyond the control of the external ISP programmer supplied by Equinox Technologies. For full details of the bug and ways to avoid it, please see the text below.

Problem: SCK pin – Lock

Symptom
You programmed code/data into the AT89S device once and it programmed correctly. Every time you then try to re-program the device, the error message 'Could not program location 0x0000' is displayed.

Description
The AT89S device requires that the 'SCK' pin is driven 'LOW' by the external ISP programmer before the device is placed into RESET mode. This means that the SCK pin must be asserted 'LOW' by the programmer while the processor is actually executing 'user firmware'. If the 'user firmware' happens to write a logic '0' to the SCK pin before the external programmer has had chance to drive the pin LOW, then the device will never re-enter 'Serial Programming Mode'.

It appears that the SPI shift register inside the AT89S device receives at least one erroneous edge on the SCK pin (hdue to an internal design problem) thereby getting out of synchronisation. As there is no way of the programmer detecting when it is in sync or not, it is impossible to get the AT89S device into programming mode. This explains why the device programmed correctly the fist time, but locks up on subsequent attempts.

How to avoid the problem

i. Avoid writing to the SCK pin for at least time 'T3'.
This basically allows the external programmer to assert SCK LOW before the 'user firmware' in the AT89S device asserts it LOW. This is effectively a race against time. If the programmer beats the 'user firmware' to asserting the SCK pin, then the device will successfully enter 'Serial Programming Mode'. If the 'user firmware' gets there before the programmer, then the device is locked from further in-system programming. It is then necessary to erase the the 'user firmware' using a using 'Parallel Programming Mode' using a suitable 'Parallel' programmer.

ii. Avoid writing to the SCK pin completely
This method ensures that the user firmware can not be in contention with the external ISP programmer.

iii. Make sure that you have used the correct RESET circuit.
The Equinox ISP programmers are set up to program AT89S target systems with a Capacitor/Resistor RESET circuit as detailed in the manual. The 'state machine' timings for getting into programming mode are shown in the 'Options -> ISP Settings' dialogue box. The timings 'T1…T6' are set for a 10uF/1K C/R RESET circuit. If these component values are not used, the programmer is unlikely to be able to get the AT89S device into 'Serial Programming Mode'.

Please note:
The correct programming operation of AT89S devices in 'Serial Programming Mode' is not guaranteed if an external 'Econoreset' or 'Watchdog RESET' device is used. These devices effectively filter out the relevant pulses which the programmer uses to place the AT89S device into programming mode.

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How to get an AT89S device which has been locked back to life

Once an AT89S device experiences the problem of not being able to re-program in serial mode, it is then impossible to even erase the device in 'Serial Programming Mode'. The only option is to remove the AT89S device from the user target system and place it in the ZIF socket of a 'parallel' programmer. If the device is erased in 'Parallel Programming Mode', the user firmware which is writing to the SCK pin will be erased and the problem should disappear. At this point, please re-check your firmware and insert a delay at the beginning of your code.

Future plans

Equinox are trying to find a way of getting around this annoying bug. As soon as we have a solution, our Meridian software will be updated.

Disclaimer

Equinox Technologies UK Ltd. can not accept any responsibility for any user target system problems arising from this bug. Please be aware when designing a target system using the Atmel AT89S Family that this bug may cause problems and there is currently no way of completely curing the problem.

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Equinox Timings for AT89S In-System Programming

Software: Meridian V2.07
Programmer: Micro-ISP Series III/IV, Activ8r (8051)

State	Time base (ms)	RESET	Processor State	SCK	MOSI	MISO	Description
0	T1	FLOAT	RUN	DR-L	DR-LOW	IP+PULL UP	Initial set up of RESET and SPI lines. Device is running code when MOSI & MISO are driven LOW.
1	T2	ACTIVE	RESET	DR-L	DR-LOW	IP+PULL UP	Assert RESET pin -> Device goes into RESET state
2	T3	FLOAT	RESET/ RUN	DR-L	DR-LOW	IP+PULL UP	De-assert RESET pin. RESET is allowed to decay naturally with user RESET circuit (ie. not driven)
3	T4	ACTIVE	RESET	DR-L	DR-LOW	IP+PULL UP	Assert RESET pin -> Device goes into RESET state. A delay of 'T4' is introduced to allow the RESET circuit to settle.
4	-	ACTIVE	RESET / SPM	DR-H/L	DR-H/L	IP+PULL UP	The programmer sends the 'Enter Serial Programming Mode' command.

Notes:

i. ACTIVE
This means that the programmer drives the RESET line HIGH or LOW. The polarity depends on the setting of the 'Reset Polarity' option in the 'ISP Settings' dialogue box within Meridian.

ii. Float
This means that the programmer effectively tri-states off the RESET line leaving it to 'float'. The target RESET circuit must therefore pull the RESET LOW (or HIGH depending on the the 'Reset Polarity' option in the 'ISP Settings' dialogue box within Meridian).

iii. RESET
The AT89S device is in the RESET state as defined by the 8051 Databook.

iv. RUN
The AT89S device is in code execution mode.

v. SPM
The AT89S device is in 'Serial Programming Mode'. The CODE/FLASH areas of the device can be programmed through the SPI port when the device is in this mode.

vi. DR-L
The pin is 'driven' LOW by the programmer.

viii. DR-H
The pin is 'driven' LOW by the programmer.

ix. DR-H/L
The pin is driven HIGH and LOW by the programmer in order to output data.

x. IP + PULL UP
The programmer pin is set to an input with a nominal 100K pull up.

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