MBX Series Embedded Controller Installation and Use

MBXA/IH1

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Preface

The *MBX Series Embedded Controller Installation and Use* manual provides general information, hardware preparation and installation instructions, operating instructions, a functional description, and various types of interfacing information for the MBX family of Embedded Controller boards.The information in this manual applies to the following MBX models.

MBX821-001	MBX860-001
MBX821-002	MBX860-002
MBX821-003	MBX860-003
MBX821-004	MBX860-004
MBX821-005	MBX860-005

This manual is intended for anyone who wants to supply OEM systems, add capability to an existing compatible system, or work in a lab environment for experimental purposes. A basic knowledge of computers and digital logic is assumed.

After using this manual, you may wish to become familiar with the publications listed in the *Related Documentation* section in Appendix A of this manual.

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Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor AC power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Lithium Battery Caution

The board contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

WARNING

This equipment generates, uses, and can radiate electro-magnetic energy. It may cause or be susceptible to electro-magnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

CE

European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 (CISPR 22) Radio Frequency Interference

EN50082-1 (IEC801-2, IEC801-3, IEC801-4) Electromagnetic Immunity

The product also fulfills EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

Contents

Chapter 1 Hardware Preparation and Installation

Chapter 2 Startup and Operation

Chapter 3 Functional Description

Chapter 4 Connector Pin Assignments

Glossary

Figures

Tables

Hardware Preparation and Installation

1

Introduction

This manual provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the MBX family of Embedded Controller boards.

MBX series boards are based on the EBX (5.75 × 8 inch) industry standard form factor specification. They provide single-board computer functionality with emphasis on open communications and networking capabilities. The features they incorporate make them well suited for applications in such areas as communications, industrial automation, and imaging.

The MBX series has two parallel branches whose differences lie in the processor that powers them: one configuration is based on Motorola's MPC821 embedded processor, while the other uses an MPC860 processor. The MPC860 version offers two additional serial communications controllers (SCCs); the MPC821 version has an integrated LCD controller in their place. In other respects, the logic design is the same for both versions.

MBX series boards are offered in ''standard'' and ''entry-level'' configurations. In either configuration, the complete MBX series embedded controller offers integral system functions as well as peripheral functions on a single base board (see the *Features* section for details). Standard configurations furnish the additional capability of PCI/ISA expansion via plug-in expansion modules.

The block diagrams in Figures 1-1 through 1-3 illustrate the architecture of MBX series embedded controllers.

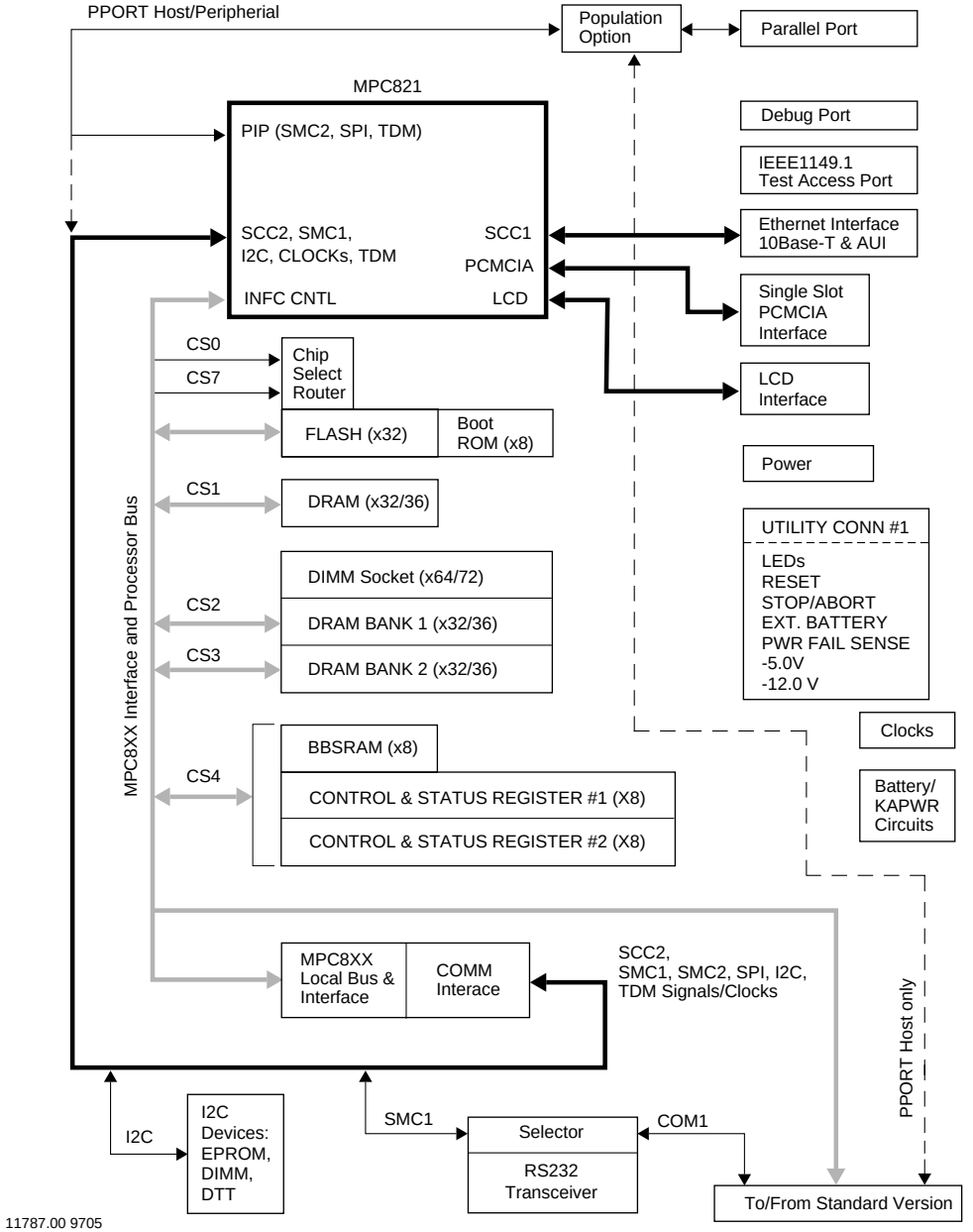


Figure 1-1. MBX821 Block Diagram (Entry-Level Version)

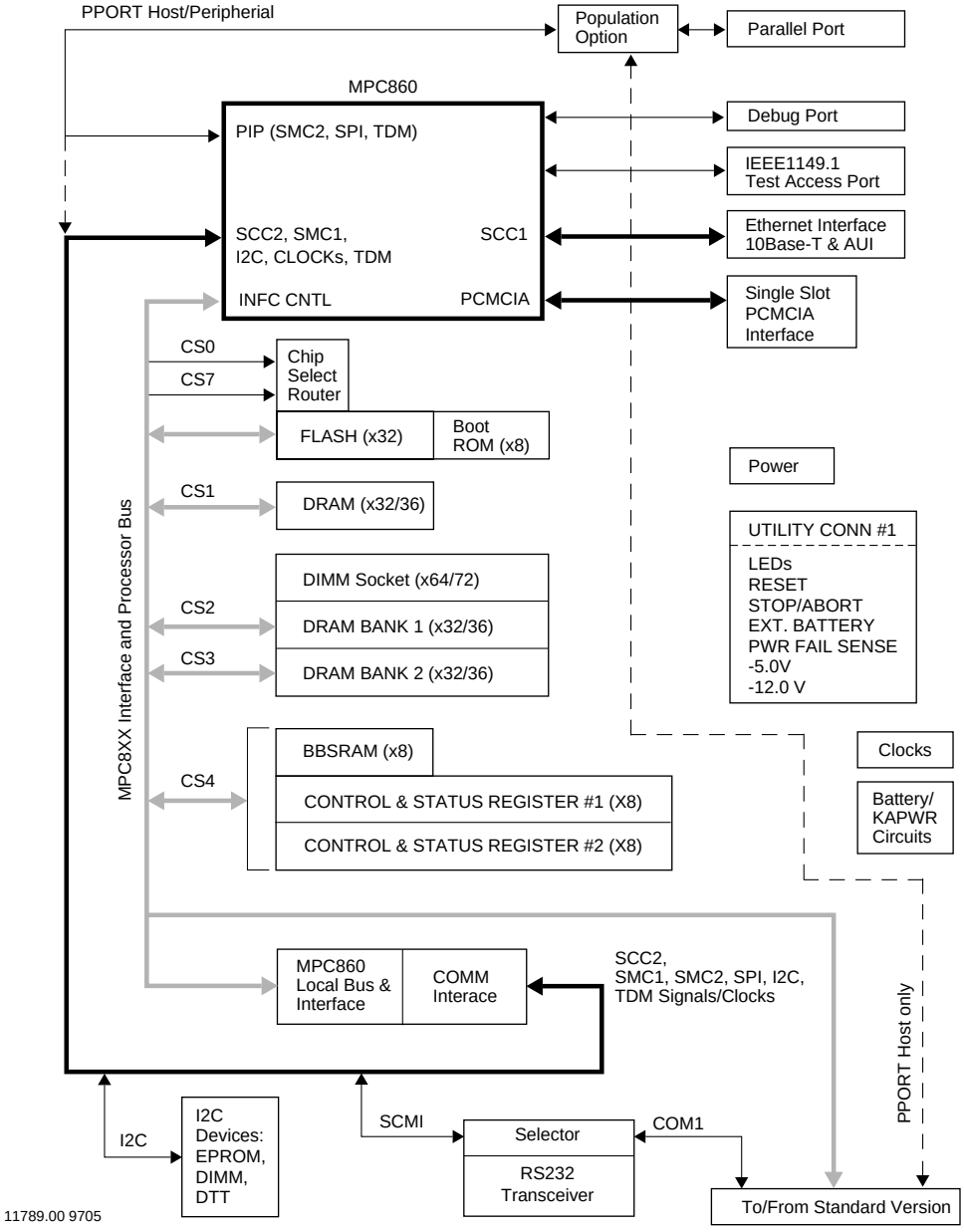


Figure 1-2. MBX860 Block Diagram (Entry-Level Version)

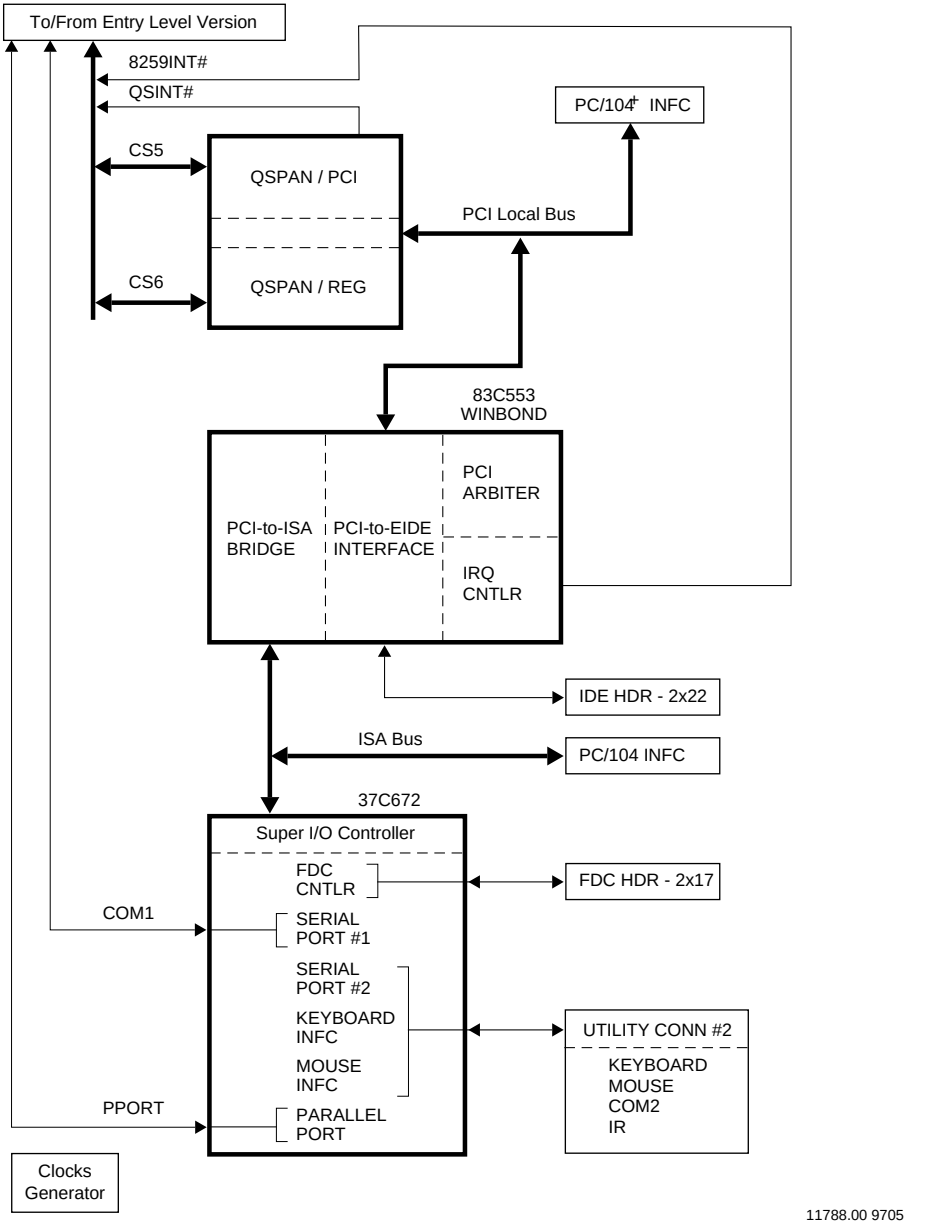


Figure 1-3. MBX821/860 Block Diagram (Standard Version)

Equipment Required

To complete an MBX system, you need the following equipment:

- Enclosure or chassis with power supply
- Display terminal
- Operating system (and/or application software)
- Disk drives (and/or other I/O) and connecting cables

The following table shows the relationship between MBX model numbers and the corresponding set of features.

Table 1-1. MBX Models

Model	Version	Description
MBX860-001	Entry	40MHz MPC860, 4MB DRAM, 2MB Flash, 10BaseT Ethernet, 32KB NVRAM, COMM interface connector.
MBX860-002	Standard	40MHz MPC860, 4MB DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, COMM interface connector.
MBX860-003	Standard	40MHz MPC860, 4MB Parity DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, parity DRAM option, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, COMM interface connector
MBX860-004	Standard	40MHz MPC860, 16MB DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, COMM interface connector
MBX860-005	Standard	40MHz MPC860, 16MB Parity DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, parity DRAM option, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, COMM interface connector
MBX821-001	Entry	50MHz MPC821, 4MB DRAM, 2MB Flash, 10BaseT Ethernet, 32KB NVRAM, LCD panel connector.
MBX821-002	Standard	40MHz MPC821, 4MB DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, LCD panel connector.
MBX821-003	Standard	40MHz MPC821, 4MB Parity DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, parity DRAM option, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, LCD panel connector
MBX821-004	Standard	40MHz MPC821, 16MB DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, LCD panel connector
MBX821-005	Standard	40MHz MPC821, 16MB Parity DRAM, 4MB Flash, PC/104-*Plus*, 10BaseT Ethernet, parity DRAM option, EIDE and Floppy interfaces, 32KB NVRAM, keyboard, mouse, IR, COM1 and COM2 ports, LCD panel connector

Overview of Startup Procedure

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

Table 1-2. Startup Overview

What you need to do...	Refer to...	On page...
Unpack the hardware.	*Unpacking Instructions*	1-8
Configure the hardware by setting jumpers on the board.	*MBX Series Embedded Controller Preparation*	1-9
Ensure expansion modules are properly installed.	*MBX Board Installation*, Expansion Modules	1-20
Install the MBX series board in a chassis and connect a display terminal	*MBX Board Installation*, MBX Board	1-23
Connect any other equipment you will be using.	*Connector Pin Assignments*	4-1
	For more information on optional devices and equipment, refer to the documentation provided with the equipment.	
Power up the system.	*Startup and Operation*	2-1
Note that the firmware initializes the board.	*EPPCBug Firmware*, Using the Debugger	5-3
	You may also wish to obtain the *PowerPC EPPCBug Firmware Package User's Manual*, listed in the *Related Documentation* Appendix.	A-1
Initialize the system clock, if necessary.	*EPPCBug Firmware*, Debugger Commands	5-4
Examine and / or change environmental parameters.	*VPD* and *ENV* commands	6-2 and / or 6-3
Program the board as needed for your applications.	*MBX Series Embedded Controller Programmer's Reference Guide*, listed in the *Related Documentation* Appendix.	A-1

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution

When unpacking, avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the MBX series embedded controller, you may need to carry out certain hardware modifications before installing the board.

The MBX series embedded controller provides software control over most options: by setting bits in control registers after installing the board in a system, you can modify its configuration. (MBX control registers are described in Chapter 3, and / or in the *MBX Series Embedded Controller Programmer's Reference Guide* as listed in the *Related Documentation* appendix.)

Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers on the MBX board.

Caution

When setting jumpers, avoid touching areas of integrated circuitry; static discharge can damage circuits.

MBX Series Embedded Controller Preparation

Figure 1-4 illustrates the placement of the jumper headers, connectors, and LED indicators on the MBX board. Manually configurable items on the board are listed below. Default settings are enclosed in brackets.

Table 1-3. Jumper Settings

Jumper	Function	Settings	
J1	Backup power configuration	1-2 [2-3]	On-board battery in. On-board battery out.
J2	Backup power conditioning	1-2 2-3 [3-4]	Initialization (breaking "freshness seal"). Not used. Normal mode.
J3	Boot ROM write protection	1-2 [2-3]	Boot ROM write protection on (writes disabled). Boot ROM write protection off (writes enabled).
J4	Boot ROM device selection	1-2 [2-3]	Port size = 8 bits; boot from ROM. Port size = 32 bits; boot from Flash.
J5	Test / Debug port selection	1-2 [2-3]	IEEE 1149 functionality enabled at IEEE 1149 header. Debug functionality enabled at Debug header.
J6	Arbitration mode	1-2 [2-3]	External arbitration selected (for one or two external masters). Internal arbitration selected (for one external master only).
J7	IDE interface configuration	1-2 [2-3]	"Native" addressing mode selected for IDE interface. "Legacy" addressing mode selected for IDE interface.
J8	DRAM DIMM configuration	[1-2] 2-3	1M / 2M / 4M x 64 / 72 DRAM DIMM (8 / 16 / 32 MB) installed. 8M x 64 / 72 DRAM DIMM (64 MB) installed.
J9	DRAM DIMM configuration	[1-2] 2-3	1M / 2M x 64 / 72 DRAM DIMM (8 / 16 MB) installed. 4M / 8M x 64 / 72 DRAM DIMM (32 / 64 MB) installed.
J10	DRAM DIMM configuration	[1-2] 2-3	1M x 64 / 72 DRAM DIMM (8 MB) installed. 2M / 4M / 8M x 64 / 72 DRAM DIMM (16 / 32 / 64 MB) installed.
J11	DREQ* signal source for DMA-type PCMCIA cards	1-2 [2-3]	PCMCIA module DREQ* signal on INPACK* pin. PCMCIA module DREQ* signal on BVD2_SPKR pin.

MBX series embedded controllers are factory tested and shipped with the default configurations listed above and described in the following sections. The MBX family's required and factory-installed debug monitor, EPPCBug, operates with those factory settings.

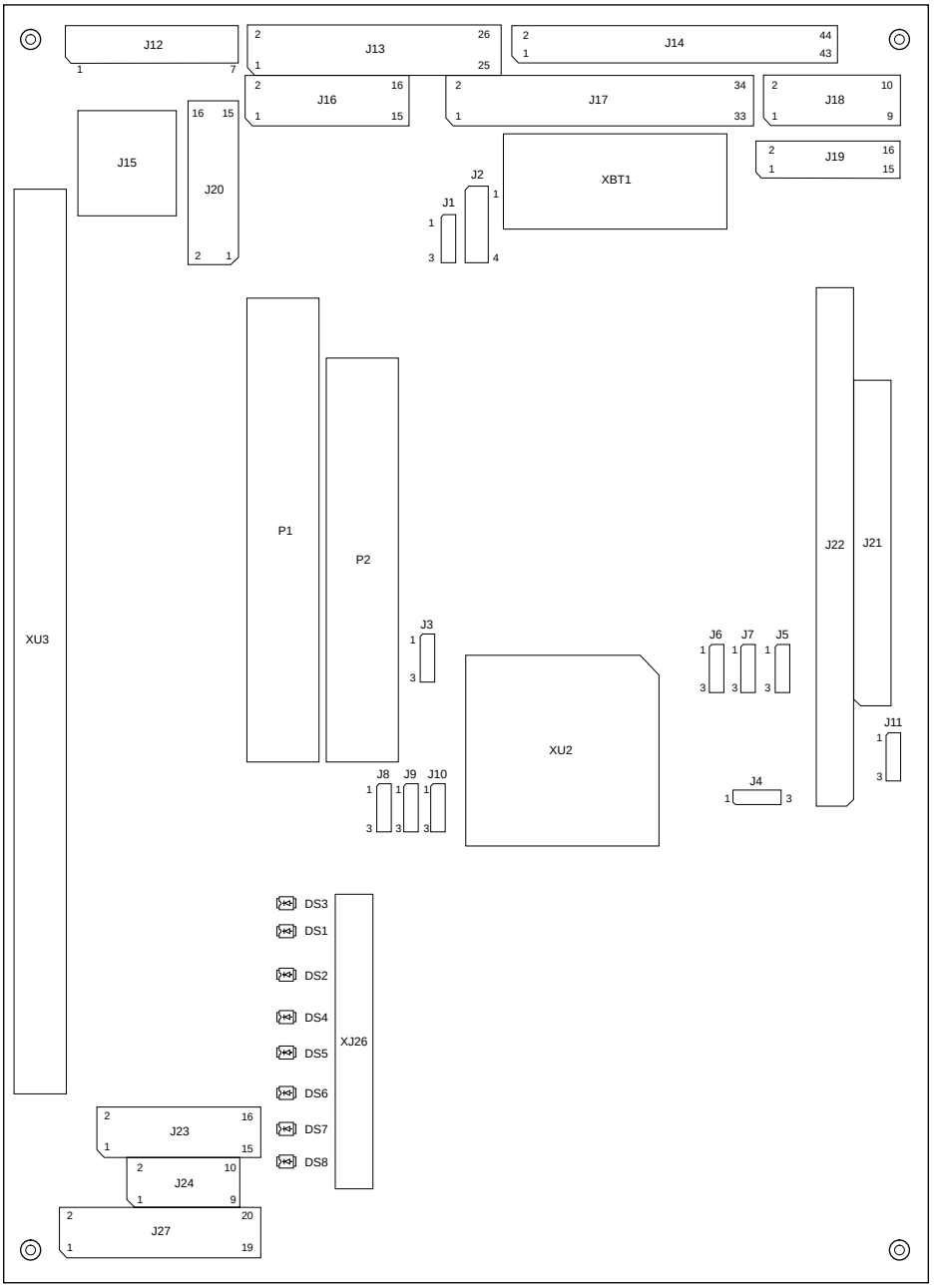


Figure 1-4. MBX821/860 Connectors, Headers, LEDs

Backup Power Configuration (J1)

MBX series embedded controllers have the capability to use 3.0V-3.6V battery power (either on-board, or external via utility connector #1) as a backup power source for the ‘‘keep-alive’’ power circuits (such as the real-time clock) in the MPC8*xx* processor.

To select either battery source as the ‘‘keep-alive’’ power source, install a jumper across J1 pins 1 and 2. If no battery is installed, or if no backup is desired, place a jumper across pins 2 and 3 (the default for shipping and storage).

Note Upon initial installation of a backup battery or upon initial receipt of the MBX board, you will need to break the battery’s ‘‘freshness seal’’. Refer to the next section for the procedure to follow.

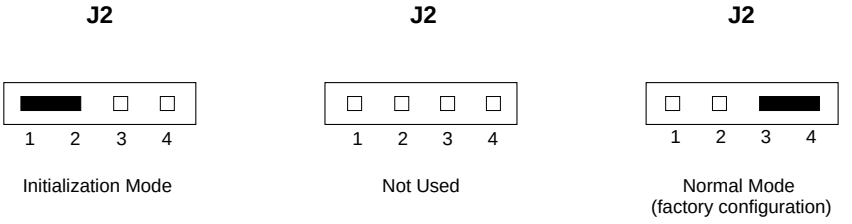
For purposes of shipping and storage, install a jumper across J1 pins 2 and 3. Upon subsequent re-use of the board, the battery’s ‘‘freshness seal’’ must be re-broken.

Backup Power Conditioning (J2)

When you install a fresh backup battery on the MBX series embedded controller (or when you place a jumper across J1 pins 1 and 2), part of the procedure involves breaking the battery's ''freshness seal'', i.e. initializing the keep-alive circuitry of the board. Jumper header J2 is provided for that purpose.

The installation procedure for on-board batteries is described in the *Hardware Installation* section. After installing the battery (or after connecting an external battery), you initialize the keep-alive circuitry as follows:

1. Turn off the power to the board.
2. Place a jumper across J2 pins 1 and 2.
3. Turn on the power to the board.
4. With power applied, move the jumper to J2 pins 3 and 4.



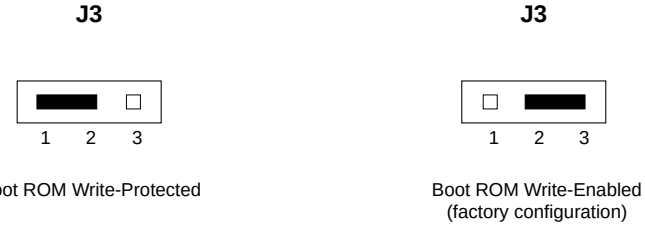
Boot ROM Write Protection (J3)

Flash memory on the MBX series embedded controller consists of one bank of four 32-pin PLCC Flash devices soldered directly to the board. Flash memory provides 2MB (in entry-level versions) or 4MB (in standard versions) of storage. EPPCBug firmware takes up 512KB (128K words) of space; the remainder of Flash memory is available for user applications. The firmware resident in Flash memory is originally loaded at the factory, but the Flash contents can be reprogrammed if necessary.

For purposes of reprogramming Flash, the MBX includes a 32-pin socket (XU2) in which firmware programmers can install a removable boot ROM device. To prevent inadvertent overwriting of the Flash memory used in the boot ROM, header J3 provides write protection for the device installed in XU2.

Installing a jumper across header J3 pins 1 and 2 protects the boot ROM against overwriting.

The factory configuration uses pins 2 and 3, so that any device present in XU2 is write-enabled.



To complete the MBX boot device configuration, you must set J4 (boot ROM device selection) on the board as well.

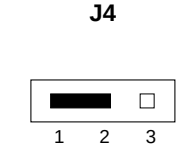
Boot ROM Device Selection (J4)

The firmware resident in Flash memory on the MBX series embedded controller is originally loaded at the factory, but the Flash contents can be reprogrammed if necessary. For purposes of reprogramming Flash, the MBX includes a 32-pin socket (XU2) in which firmware programmers can install a removable boot ROM device.

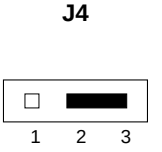
As described under *Boot ROM Write Protection*, header J3 provides write protection for the device installed in XU2 to prevent inadvertent overwriting of the Flash memory used in the boot ROM. J4 enables you to select either the on-board Flash memory (x32) or the socketed Flash chip in XU2 (x8) as the boot ROM. As a secondary function, J4 defines the bus width of the device selected — 8 bits for the socketed Flash, 32 bits for the on-board Flash.

To select the ROM in socket XU2 as the boot device at power-up, jumper J4 pins 1 and 2. To select the on-board Flash as the power-up boot device, jumper J4 pins 2 and 3.

The factory configuration uses pins 2 and 3, so that the on-board Flash serves as boot device during power-up resets.



Boot Port = 8 bits / ROM



Boot Port = 32 bits / Flash
(factory configuration)

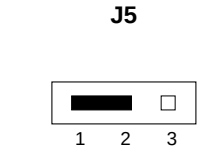
Test/Debug Port Selection (J5)

As described in Chapter 3, certain MPC821 and MPC860 signal lines have a dual function on the MBX series embedded controller: they may serve either as IEEE 1149 test port signals or as Debug port signals, depending on jumper settings. Jumper J5 regulates the state of those signal lines as shown below:

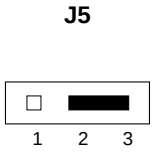
Table 1-4. Pin Definitions — IEEE 1149/Debug Port Signals

MPC8xx Pin	IEEE 1149 Signal	Debug Signal
H16	TCK	DSCK
H17	TDI	DSDI
G17	TDO	DSDO

Placing a jumper on J5 pins 1-2 configures the MPC8*xx* pins listed above as IEEE 1149 test port signals and enables IEEE 1149 functionality at the Test Port header (J23 on the MBX board).



IEEE 1149 Test Port Enabled



Debug Port Enabled
(factory configuration)

Placing a jumper on J5 pins 2-3 (the factory default) configures the MPC8*xx* pins listed above as Debug port signals and enables that functionality at the Debug Port header (J24 on the MBX board).

The pin assignments of the IEEE 1149 and Debug Port headers are listed in Chapter 4.

For additional details on the configuration and use of the multiplexed IEEE 1149 test port and Debug port signals, refer to the *MBX Series Embedded Controller Programmer's Reference Guide* (listed in the *Related Documentation* appendix).

Arbitration Mode (J6)

The MBX series embedded controller supports an *internal* and an *external* system arbitration mode.

- The internal setting allows one extra master besides the MPC8*xx* processor. On standard boards, the additional master would be the QSPAN PCI host bridge. On entry-level boards, the additional master would be an add-on MPC8*xx*-type daughter card on the MPC8*xx* bus.
- The external setting allows two masters in addition to the MPC8*xx* processor. The additional masters would be both the QSPAN PCI host bridge and a card on the MPC8*xx* bus.

Note Given the guidelines set forth above, external arbitration is restricted to standard-level boards with an add-on MPC8*xx*-type daughter card capable of bus master operation.

Placing a jumper on J6 pins 1-2 configures the MBX for external arbitration. Placing a jumper on J6 pins 2-3 (the factory default) configures the MBX for internal arbitration.

IDE Interface Configuration (J7)

IDE (Integrated Drive Electronics) I/O controllers can be categorized as either ‘‘legacy’’ or ‘‘native’’ devices. ‘‘Legacy’’ devices use a hard-wired addressing scheme with fixed interrupt requests. The more recent ‘‘native’’ devices use controller registers that are relocatable in I/O space, with interrupt requests mapped to the appropriate registers.

Use J7 to configure the IDE interface on MBX series boards as necessary for the devices you have installed.

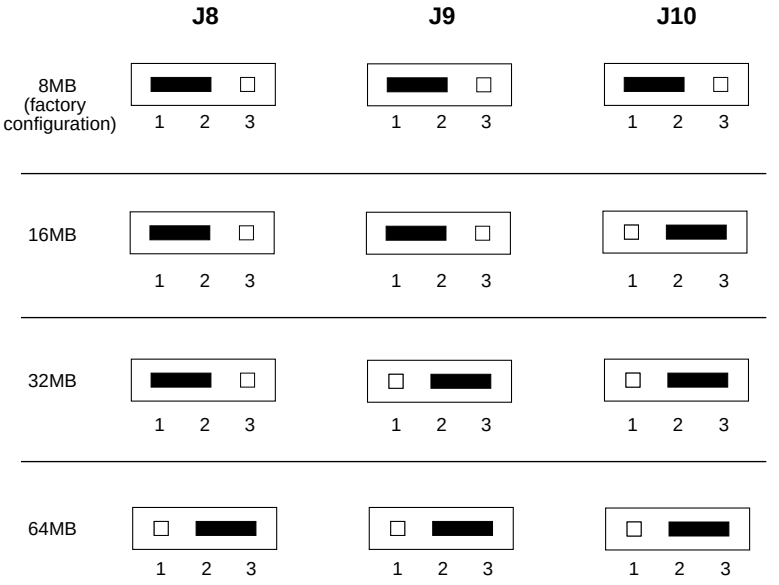
Placing a jumper on J7 pins 1-2 configures the IDE interface for native addressing mode. Placing a jumper on J7 pins 2-3 (the factory default) configures the IDE interface for legacy addressing mode.

For additional details on programming IDE devices, refer to the *MBX Series Embedded Controller Programmer's Reference Guide* (listed in the *Related Documentation* appendix).

DRAM DIMM Size (J8-J10)

The MBX series embedded controller has provision for either 4MB or 16MB of on-board DRAM, soldered in place. In addition, it accommodates 8MB to 64MB of expansion DRAM in a 168-pin DIMM (dual in-line memory module) socket, XU3.

J8, J9, and J10 are configured as a set to match the size of the DRAM module you have installed on the MBX. Set the jumpers as shown below to configure the MBX for 8MB, 16MB, 32MB, or 64MB of expansion DRAM in socket XU3.



DREQ# Signal Source for DMA-type PCMCIA Cards (J11)

A single-slot PCMCIA interface (using socket XJ26) and controller are available on the MBX series embedded controller. The interface is configurable for DMA- versus non-DMA PCMCIA cards, in that the routing of the INPACK# signal (needed only for some cards with DMA capability) can be defined.

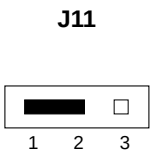
If you are installing a PCMCIA card with DMA capability, the routing of the PCMCIA INPACK# signal needs to be defined via jumper header J11. Refer to the PCMCIA vendor documentation for specifics on the card you intend to install; if the DREQ# signal is routed via INPACK# or BVD2_SPKR, set J11 as indicated in the following table.

For non-DMA cards, place a jumper on J11 pins 2-3 to permit use of the BVD2_SPKR signal.

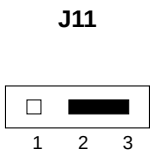
Table 1-5. DREQ# Signal Routing

If PCMCIA Card is...	And DREQ# Signal is...	Jumper J11 Pins...
DMA type	On INPACK#	1-2
	On BVD2_SPKR	2-3
Non-DMA type	N / A	2-3

The factory configuration uses pins 2-3 on J11.



DREQ# Signal on INPACK# Pin



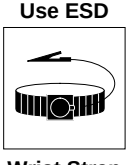
DREQ# Signal on BVD2_SPKR Pin
(factory configuration)

MBX Board Installation

The following sections describe the installation of the MBX series embedded controller in an enclosure and discuss the system considerations relevant to the installation. Before mounting expansion modules and installing the MBX, ensure that all user-configurable jumpers on the board are configured as necessary. Not all the jumper headers are easily accessible with expansion modules installed.

In many cases, the expansion modules—the PC/104 (ISA), PC/104-*Plus* (PCI), and the 8xx/COMM boards for additional expansion if applicable—are already in place on the MBX. Should it be necessary to install expansion modules on the base board, refer to the following sections for a brief description of the installation procedure.

ESD Precautions



Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

Expansion Modules

PC/104 (ISA), PC/104-*Plus* (PCI), 8xx/COMM, and PCMCIA expansion modules plug into the top of the MBX board. To install an expansion module, refer to Figure 1-4 and proceed as follows. No tools are necessary for this procedure.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the card cage.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. If the MBX series embedded controller is presently installed in a system, carefully remove the board from its mounting location. (Reverse the MBX installation procedure described in the next section.)
4. Lay the board flat on a static-free surface.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

5. Referring to Figure 1-4, locate the connector(s) provided for expansion modules on the MBX board:
   - PC/104 (ISA) and PC/104-*Plus* (PCI) modules plug into J21 and J22 in tandem at one end of the module; they use P2 at the other end of the module.
   - 8xx/COMM modules plug into P1.
   - PCMCIA modules plug into XJ26.

6. Seat the expansion module firmly and evenly in the appropriate connector(s) as shown in Figure 1-5. The plug on the underside of the expansion module should connect smoothly with the corresponding socket on the MBX board.

Note If you add an 8xx / COMM expansion module (user-supplied), it must be installed first; PC / 104 / PC / 104-*Plus* modules stack on top of it. You can stack up to three PC / 104 / PC / 104-*Plus* modules on the MBX.

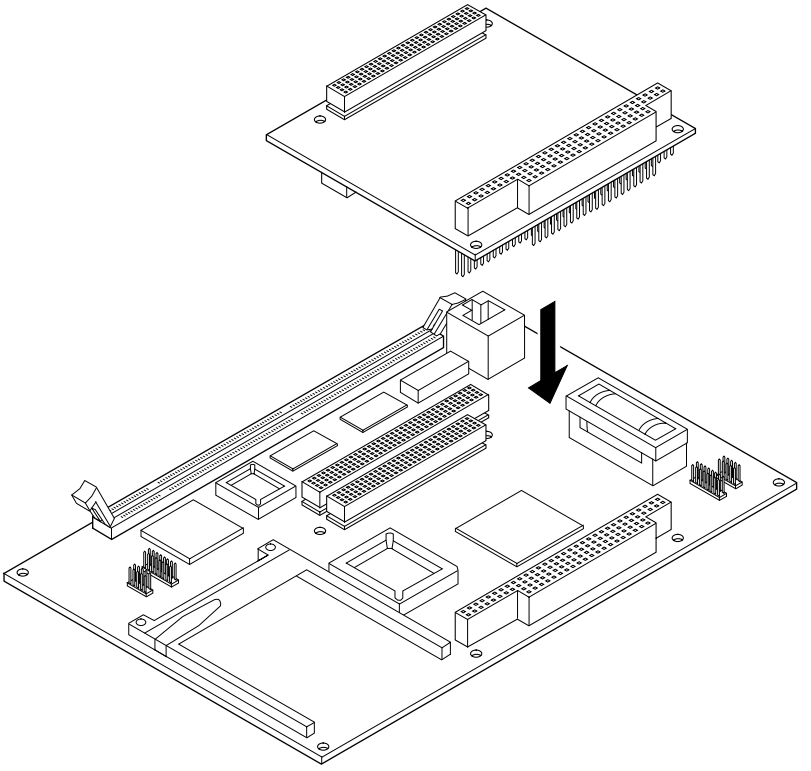


Figure 1-5. Installing Expansion Module on MBX Board

MBX Board

With expansion module(s) installed and jumper headers properly configured, proceed as follows to install the MBX board in an enclosure (user-supplied). You need a Phillips screwdriver for this procedure. Depending on how the MBX board-to-chassis standoffs are installed, you may need a hex nut driver, typically 3/16-inch, as well.

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the card cage.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. If the MBX board-to-chassis standoffs are not already installed in the enclosure, insert the standoffs through the holes drilled for that purpose in the chassis. Secure the standoffs with the nut driver or screwdriver as appropriate.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

4. Place the MBX board on the standoffs.
5. Insert four short Phillips screws through the holes at the corners of the MBX board, into the standoffs you installed in the chassis. Tighten the screws.

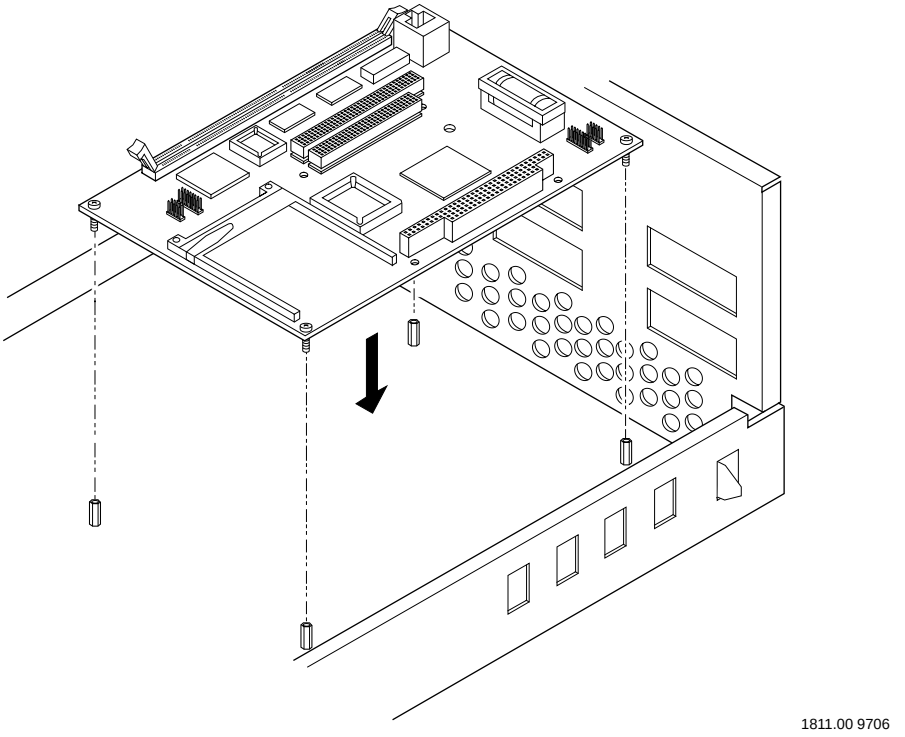


Figure 1-6. MBX Board Installation in Chassis

6. Connect the power and peripheral cables to the MBX board as appropriate for your system configuration.
7. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

On the MBX series embedded controller, the standard serial console port serves as the firmware console port. The firmware console should be set up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

9600 baud is the power-up default for serial ports on MBX series boards. After power-up you can reconfigure the baud rate if you wish, using the EPPCBug **PF** (Port Format) command via the command line interface. Whatever the baud rate, some type of hardware handshaking — either XON / OFF or via the RTS / CTS line — is desirable if the system supports it.

Startup and Operation 2

Introduction

This chapter supplies information on use of the MBX series embedded controller in a system configuration. Here you will find descriptions of the switches and LEDs, the power-up procedure, and the firmware initialization process.

Switches and LEDs

The MBX board has provision for user-installed Abort and Reset switches and includes eight on-board LED (light-emitting diode) status indicators. The switches and six additional LED signals (five for Ethernet activity and one for an external hard disk drive) are available remotely via utility connector #1 (J16 on the MBX board).

ABORT Switch

When activated by software, the Abort switch can generate an interrupt signal to the MPC8*xx* processor at the IRQ7 level. The interrupt can be programmed as falling-edge active or as low-level active. The circuit is filtered for noise, to prevent false aborts.

RESET Switch

The Reset switch resets all onboard devices, including the PC/104, PC/104-*Plus*, and 8*xx*/COMM ports and the KAPWR (keep-alive power) circuits.

LED Indicators (DS1 - DS8)

There are eight status LEDs on the MBX board. As mentioned at the beginning of this section, six additional LED signals (five for Ethernet activity and one for an external hard disk drive) are available for external display via utility connector #1 (J16 on the MBX board). The LEDs on the board have the functions listed below.

Table 2-1. On-Board LEDs

LED	Status at Reset	Function
DS1 (green)	Off	CPU activity; lights when the MPC8*xx* processor bus is active. Should extinguish when board is reset.
DS2 (green)	Off	PCI activity; lights when the PCI bus is active. Valid only on standard versions of the MBX board; should remain off on entry-level versions.
DS3 (yellow)	On	Status LED #1; available for user applications
DS4 (yellow)	On	Status LED #2; available for user applications
DS5 (green	On	+3.3Vdc OK; lights when +3.3Vdc power is available on the MBX board.
DS6 (green)	On	+5Vdc OK; lights when +5Vdc power is available on the MBX board.
DS7 (green)	On	+12Vdc OK; lights when +12Vdc power is available on the MBX board.
DS8 (orange)	On	Board failure; lights when a fault is present on the MBX board.

Note It is possible to employ DS3, DS4, and DS8 as a group to generate a binary indication of board status for user-specific applications. For details, refer to the *MBX Series Embedded Controller Programmer's Reference Guide.*

Initial Conditions

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. Applying power (as well as resetting the system) triggers an initialization of the MPU, the hardware, and the firmware.

The firmware initializes the devices on the MBX board in preparation for booting the operating system. The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system. For further information on the firmware, refer to Chapter 5, *EPPCBug Firmware*; or to the *PowerPC EPPCBug Firmware Package User's Manual.*

Pre-Startup Check

Before you power up the MBX system, be sure that the following conditions exist:

1. Jumpers and/or configuration switches on the MBX and associated equipment are set as required for your particular application.
2. The EPPCBug boot ROM is known to be present in socket XU2 on the top side of the MBX board (if booting from the socketed device); or the EPPCBug firmware is known to be installed in the Flash devices on the secondary side of the board (if booting from 32-bit Flash).
3. The MBX board is installed and cabled up as appropriate for your particular chassis or system, as outlined in Chapter 1.
4. The terminal that you plan to use as the EPPCBug system console is connected to the EIA-232-D console port (J18 on the MBX board).
5. The terminal is set up as follows:
   - Eight bits per character
   - One stop bit per character
   - Parity disabled (no parity)
   - Baud rate 9600 baud (default baud rate of MBX ports at power-up)

6. Any other device you wish to use, such as a host computer system and / or a parallel printer, is cabled to the appropriate header.

Notes After power-up you can, if you wish, reconfigure the serial ports by programming the MBX console interface, or by using the EPPCBug Port Format (**PF**) command.

In order for high-baud-rate serial communication between EPPCBug and the terminal to work, the terminal must do some form of handshaking. If your terminal does not do hardware handshaking via the CTS line, then it must do XON / XOFF handshaking. If you get unintelligible messages and missing characters, check the terminal to be sure that XON / XOFF handshaking is enabled.

After you complete the checks listed above, you are ready to power up the system.

Applying Power

When you power up (or reset) the system, EPPCBug executes some self-checks and proceeds to the hardware initialization. The following hardware components are initialized at power-up / reset:

- MPC821 / 860 PowerPC Core
- MPC821 / 860 System Interface Unit (SIU)
- MPC821 / 860 Memory Controller and Memory
- Primary PCI Bus Bridge Device (QSpan)
- ISA Bus Bridge Device (Winbond W83C553F)
- Super I / O Device (SMC 37C672)

- PCI Device Configuration (PCI I/O and PCI Memory Address Spaces)
- PCMCIA Module Configuration
- I/O and Memory Address Map

The system startup flows in a predetermined sequence, following the hierarchy inherent in the hardware. The figure below charts the flow of the basic initialization sequence that takes place during PowerPC system startup.

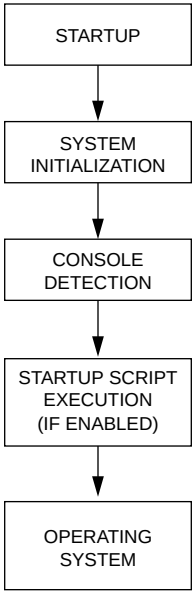


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Figure 2-1. PowerPC Firmware System Startup

2

Restarting the System

You can initialize the system to a known state in two different ways: reset or break. Each method has characteristics that make it more appropriate than the others in certain situations.

Reset

Powering up the MBX Series board initiates a system reset. Resets can also be asserted through the Reset switch, available remotely via utility connector #1 (J16 on the MBX board). Both ‘‘cold’’ and ‘‘warm’’ reset modes are available. By default, EPPCBug is in ‘‘cold’’ mode (refer to the RESET command description in the *PowerPC EPPCBug Firmware Package User’s Manual*).

During cold resets, these system initialization processes occur, as if the MBX had just been powered up:

- All static variables are restored to their default states.
- Breakpoint table and offset registers are cleared.
- Target registers are invalidated.
- Input and output character queues are cleared.
- Onboard devices are reset, and the console/terminal serial port is reconfigured to its default state.

During warm resets, the EPPCBug variables and tables are preserved, as are the target state registers and breakpoints.

Note Early revisions of the EPPCBug do not support the ‘‘warm’’ reset feature.

You need to reset the system if the processor ever halts or if the EPPCBug environment is ever lost (vector table destroyed, stack corrupted, etc.).

Break

To invoke a break, press and release the BREAK key on the terminal keyboard. Breaks do not generate an interrupt. The only time a break is recognized is when characters are sent or received by the console port. A break removes any breakpoints in the user code and keeps the breakpoint table intact. A break also takes a snapshot of the machine state if the function was entered using SYSCALL (refer to the SYSCALL command description in the *MBX Series Embedded Controller Programmer's Reference Guide*). This machine state is then accessible to you for diagnostic purposes.

Occasionally, you may wish to terminate a debugger command before its completion (for example, during the display of a large block of memory). A break allows you to terminate the command.

For details on the firmware or the programming aspects of using the MBX series embedded controller, refer to the *PowerPC EPPCBug Firmware Package User's Manual* or to the *MBX Series Embedded Controller Programmer's Reference Guide* respectively.

Functional Description 3

Introduction

This chapter describes the MBX series embedded controller on a block diagram level. The *General Description* provides an overview of the MBX board, followed by a detailed description of several blocks of circuitry. Figure 3-1 shows a block diagram of the overall board architecture.

Detailed descriptions of other MBX blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *Programmer's Reference Guide* (listed in the *Related Documentation* section). Refer to it for a functional description of the MBX series embedded controller in greater depth.

Features

The following table summarizes the characteristics of MBX series boards. Features pertaining to both entry-level and standard versions are listed in the *upper* section. Additional features offered by the standard version alone appear in the lower section.

Table 3-1. Features of the MBX Series Embedded Controller

Feature	Description
Microprocessor	MPC860 PowerQUICC or MPC821 processor with integrated MMU and communications functions
DRAM	4MB (with optional parity) on-board DRAM; 168-pin DIMM socket addresing up to 64MB DRAM
Flash Memory	One bank (2MB 32-bit Flash) soldered to board
NVRAM	32KB NVRAM with battery backup and low battery indication
Real-time clock	RTC, watchdog timer, four 16-bit timers in MPC8*xx*
Switches	Reset and Abort, available remotely via utility connector

Table 3-1. Features of the MBX Series Embedded Controller (Continued)

Feature	Description
Status LEDs	Eight: CPU, PCI, Status #1, Status #2, +3.3Vdc, +5Vdc, +12Vdc, Board Failure
Serial I/O	EIA-232-D serial console or terminal port (DCE/DTE)
Parallel I/O	IEEE 1284 parallel port with host/peripheral mode selection
Ethernet I/O	Support for AUI and 10Base-T Ethernet interface
PCMCIA interface	One PCMCIA slot (type I, II, or III)
LCD interface (MPC821 only)	Support for both active and passive LCD panels via 20-pin header on MPC821-powered MBX boards
Communications I/O	MPC8*xx* communications interface with Time Slot Allocator (TSA) and Time Division Multiplexing (TDM) channel to support multiplexed as well as non-multiplexed serial I/O. Serial Communication Controllers (SCCs) 2-4, Serial Management Controllers (SMCs) 1-2, Serial Peripheral Interface (SPI), and Interprocessor-Integrated Controller (I^2C) signals are available. MPC8*xx* bus interface, with signals routed to same board connector as the MPC8*xx* communications interface. I/O point for other MPC8*xx*-type masters, and for TDM interfaces needing bus access.
Additional Features — Standard Version	
DRAM	Up to 16MB (with optional parity) on-board DRAM
Flash Memory	One bank 32-bit Flash (4MB total) soldered to board
PC/104-*Plus* interface	Support for PC/104 (ISA) and PC/104-*Plus* (PCI) expansion modules
EIDE port	Support for direct ribbon cable connection to $2^1/_2$-inch hard disk drive via header on MBX board; PCI bus master capability
Serial I/O	Two additional EIA-232-D serial ports
Floppy disk controller	Support for direct ribbon cable connection to 2.88MB floppy disk drive via header on MBX board
Keyboard/mouse interface	Support for keyboard and mouse input via header on MBX board

General Description

MBX series boards are a family of small form factor (5.75 × 8 inch) embedded controllers. They provide single-board computer functionality with emphasis on open communications and networking capabilities. They offer open interfaces such as PCI, ISA, and PCMCIA in addition to Ethernet and serial / parallel I / O. The features they incorporate make them well suited for embedded real-time applications in such areas as communications, industrial automation, and electronic imaging.

The MBX series has two parallel branches whose differences lie in the processor that powers them: one configuration is based on Motorola's MPC821 embedded processor, while the other uses an MPC860 processor. The MPC860 version offers two additional serial communications controllers (SCCs) than the MPC821; the MPC821 version has an integrated LCD controller in their place. In other respects, the logic design is the same for both versions.

MBX series boards are offered in ''standard'' and ''entry-level'' configurations (Table 3-1 lists the features of each). In either configuration, the complete MBX series embedded controller offers integral system functions as well as peripheral functions on a single base board. Standard configurations furnish the additional capability of PCI / ISA expansion via plug-in expansion modules.

As shown in the *Features* section, the MBX series embedded controller offers many standard features desirable in a computer system—such as synchronous and asynchronous serial ports, parallel port, boot ROM and DRAM, PCMCIA capability, Ethernet, support for external disk drives, and keyboard and mouse support—in a small, EBX form factor package. Its flexible mezzanine architecture allows relatively easy upgrades in memory and functionality.

A key feature of the MBX series family are the PCI (Peripheral Component Interconnect) and ISA (Industry Standard Architecture) bus extensions available on MBX boards in the ''standard'' configuration. ISA (also called PC / 104) and PCI (also called PC / 104-*Plus*) modules offer numerous possibilities for I / O

expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode), graphics, Ethernet, or SCSI ports. The MBX base board allows PC/104-*Plus* cards with a 32-bit, 33MHz PCI interface to be used on the same stack as PC/104 cards. (You can stack up to three PC/104/PC/104-*Plus* modules on the MBX.)

Block Diagram

Figure 3-1 diagrams the overall architecture of the MBX series embedded controller.

Processor

The MPC8*xx* processor chip used on MBX series boards is either an MPC860 PowerQUICC™ (Quad Integrated Communications Controller) or an MPC821 Portable Systems microprocessor. The processor is surface-mounted to the MBX board. The MPC8*xx* is a single-chip microprocessor/periphal combination that lends itself to a variety of controller applications. It incorporates on-chip many of the communications/networking capabilities and peripheral I/O functions offered by the overall MBX product.

MPC860

The MPC860 processor is especially well-suited for applications involving communications and networking systems. The CPU on the MPC860 is a 32-bit PowerPC™ implementation incorporating memory management units (MMUs) and instruction/data caches. It has a communications processor module that includes an Interprocessor-Integrated Controller (I^2C) channel for data exchanges between the MPC860 and other ICs with I^2C capability — microcontrollers, LCD displays, real-time clock devices, etc. The MPC860's memory controller supports all available types of memory. Its PCMCIA controller supports up to two PCMCIA sockets (one is implemented on the MBX) and a real-time clock.

MPC821

The MPC821 processor is especially well-suited for applications where lower power is essential, such as portable and / or high-performance communications systems. The CPU on the MPC821 is a 32-bit PowerPC™ implementation incorporating memory management units (MMUs) and instruction / data caches. It has a communications processor module that includes:

- Two serial communication controller (SCC) channels
- Two serial management channels (SMCs)
- A serial peripheral interface (SPI) channel
- an Interprocessor-Integrated Controller (I^2C) channel for data exchanges between the MPC821 and other ICs with I^2C capability — microcontrollers, LCD displays, real-time clock devices, etc.

The MPC821's memory controller supports all available types of memory. Its PCMCIA controller supports up to two PCMCIA sockets (one is implemented on the MBX). There is also a display capability via LCD controller and a real-time clock.

DRAM

The MBX series embedded controller has provision for either 4MB or 16MB of on-board DRAM, soldered in place. In addition, it accommodates 8MB to 64MB of expansion DRAM in a 168-pin DIMM (dual in-line memory module) socket, XU3.

The on-board DRAM is composed of two 16-bit devices (either 1M x 16 or 4M x 16). Parity protection is optional.

If expansion DRAM is installed in the DIMM socket, it must have the same characteristics as the on-board DRAM: single bank, 3.3V, EDO (extended data out), 4K refresh rate, and same clock speed.

Flash Memory

Flash memory on the MBX series embedded controller consists of 2MB (on entry-level versions) or 4MB (on standard versions) of EPPCBug firmware resident in one bank of four devices soldered directly to the board. The firmware resident in Flash memory is originally loaded at the factory, but the Flash contents can be reprogrammed if necessary.

The on-board monitor / debugger, EPPCBug, resides in the Flash chips. The EPPCBug firmware provides functionality for:

- Booting and resetting the system
- Initializing a request
- Displaying and modifying configuration variables
- Running self-tests and diagnostics
- Updating firmware ROM

For purposes of reprogramming Flash, the MBX includes a 32-pin socket (XU2) in which firmware programmers can install a removable boot ROM device. A jumper header (J4) enables you to select either the on-board Flash memory or the socketed Flash chip in XU2 as the boot ROM. Depending on the configuration of J4, resets execute either from the on-board Flash memory bank (32-bit Flash) or from the socketed boot ROM (8-bit Flash).

In normal operation, the Flash devices are in “read-only” mode, their contents are predefined, and they are protected against inadvertent writes arising from power outages. However, for programming purposes, programming voltage is always supplied to the devices and the Flash contents may be modified by executing the proper program command sequence. Refer to the third-party data sheet and / or to the *PowerPC EPPCBug Firmware Package User’s Manual* for further device-specific information on modifying Flash contents.

NVRAM

The MBX series embedded controller accommodates 32KB of non-volatile RAM (NVRAM) in a 34-pin socket, XU1. A battery supplies V_{cc} to the NVRAM when main power is removed. The NVRAM provides for a low-battery indication which can be read by the MPC8*xx* processor (via status register #2 — see *Programmer's Reference Guide*) so that you can replace the battery before it discharges completely.

About the Battery

The on-board backup power source for the NVRAM is a Sanyo CR14250SE lithium battery which is socketed for easy removal and replacement. A small capacitor is provided to allow the battery to be quickly replaced without data loss.

The lifetime of the battery is very dependent on the ambient temperature of the board and the power-on duty cycle. At 70˚C, the worst-case elapsed time for battery protection is 7 years. Battery warning time is 24 hours minimum. At lower ambient temperatures the backup time is greatly extended.

When a board is stored, the battery should be disconnected to prolong battery life. This is especially important at high ambient temperatures. The MBX board is shipped with the on-board battery disconnected (i.e., with a jumper installed across J1 pins 2 and 3). If you intend to use the battery as a backup power source, it is necessary to reconfigure the jumpers on J1 and J2 before installing the board. Refer to *Backup Power Configuration* and *Backup Power Conditioning* in Chapter 1 for the jumper configurations to use.

Warning

Lithium batteries incorporate inflammable materials such as lithium and organic solvents. If lithium batteries are mistreated or handled incorrectly, they may burst open and ignite, possible resulting in injury and / or fire. When dealing with lithium batteries, carefully follow the precautions listed below in order to prevent accidents.

- Do not short-circuit.
- Do not disassemble, deform, or apply excessive pressure.
- Do not heat or incinerate.
- Do not apply solder directly.
- Do not use different models, or new and old batteries together.
- Do not charge.
- Always check proper polarity.

To remove the battery from the module, carefully pull the battery from the socket.

Before installing a new battery, ensure that the battery pins are clean. Note the battery polarity and press the battery into the socket. When the battery is in the socket, no soldering is required.

Real-Time Clock/Timer Functions

The MPC8*xx* processor chip used on MBX series embedded controllers incorporates a clock module to provide the various system clock and timer functions as well as low power control circuitry for the system. Among the outputs of the clock module is a real-time clock (RTC). The real-time clock provides a time-of-day indication to the operating system and to application software.

The clock is unaffected by Reset signals and operates in all low-power modes. It can be programmed to generate a maskable interrupt via an alarm register. The RTC furnishes seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29- (leap year), and 30-day months are made automatically.

The MPC8*xx* processor incorporates a number of other timer functions that, on other boards, often require external circuits:

- Bus access monitor. Generates a bus error signal if accesses to the processor bus are not handled within a programmed time limit.
- Software watchdog timer. Supplies time-out protection in case of hardware or software module faults (produces a reset if software does not service a fault within a programmed space of time).
- Periodic interrupt timer. Generates interrupts at prescribed intervals for use with real-time operating systems or application software.
- Time base counter. Employs the 64-bit counter defined in PowerPC architecture as a time base reference for operating systems or application software.
- Decrementer counter. Uses the 32-bit counter defined in PowerPC architecture to generate a decrementer interrupt.

For detailed programming information and details on MPC8*xx* timer functions, refer to the *MBX Series Embedded Controller Programmer's Reference Guide.*

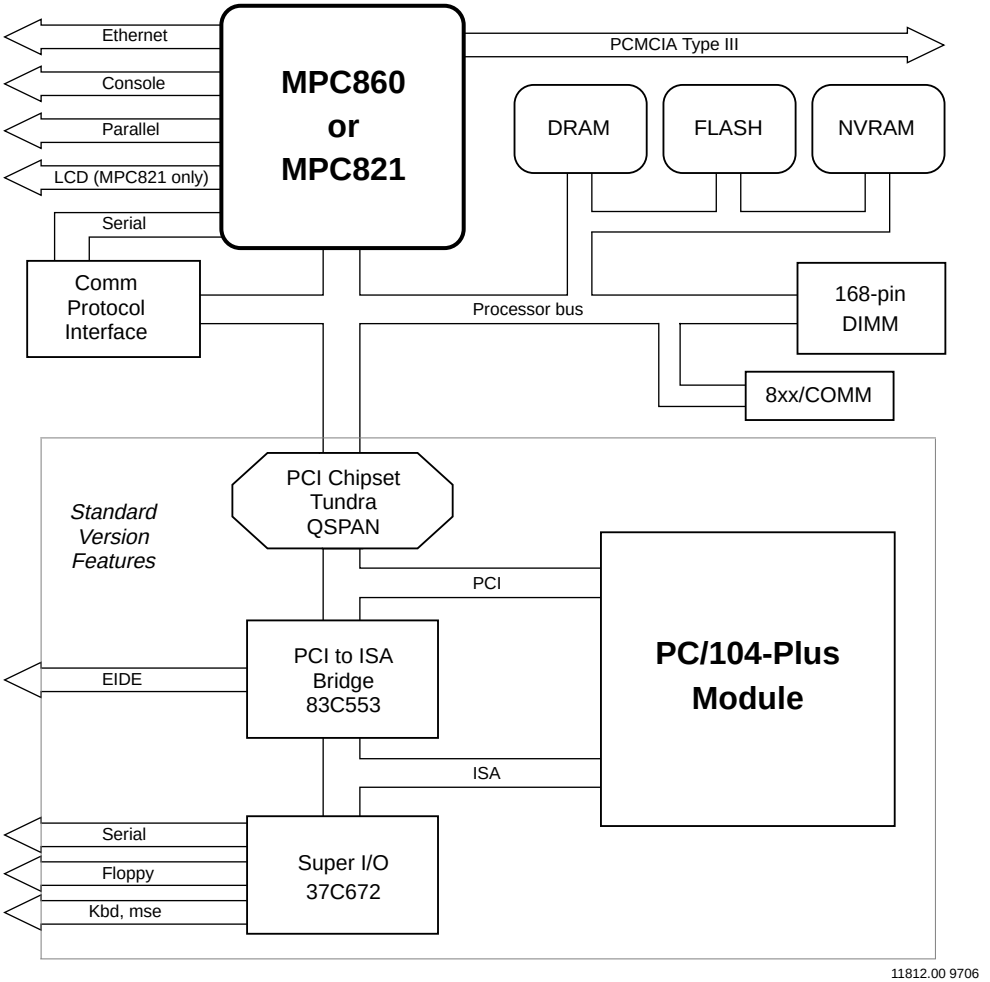

Figure 3-1. MBX Series Embedded Controller Architecture

Switches and LEDs

The MBX board has provision for user-installed Abort and Reset switches and includes eight LED (light-emitting diode) status indicators. The switches and LEDs are available remotely via utility connector #1 (J16 on the MBX board).

Abort Switch

When activated by software, the Abort switch can generate an interrupt signal to the MPC8*xx* processor at the IRQ7 level. The interrupter connected to the Abort switch is an edge-sensitive circuit, filtered to remove switch bounce.

Reset Switch

The Reset switch resets all onboard devices, including the PC/104, PC/104-*Plus*, and 8*xx*/COMM ports and the KAPWR (keep-alive power) circuits.

LED Indicators (DS1 - DS8)

Eight status LEDs are on the MBX board. As mentioned at the beginning of this section, six additional LED signals (five for Ethernet activity and one for an external hard disk drive) are available for external display via utility connector #1 (J16). The LEDs on the board have the functions listed below:

- DS1 (green). CPU activity; lights when the MPC8*xx* processor bus is active. Should extinguish upon board reset.
- DS2 (green). PCI activity; lights when the PCI bus is active. Valid only on standard versions of the MBX board; should remain off on entry-level boards.
- DS3 (yellow). Status LED #1; available for user applications.
- DS4 (yellow). Status LED #2; available for user applications.
- DS5 (green). +3.3Vdc OK; lights when +3.3Vdc power is available on the MBX board.
- DS6 (green). +5Vdc OK; lights when +5Vdc power is available on the MBX board.
- DS7 (green). +12Vdc OK; lights when +12Vdc power is available on the MBX board.
- DS8 (orange). Board failure; lights when a fault is present on the MBX board.

37C672 Super I/O Device

The MBX series embedded controller uses a 37C672 Super I/O controller chip from Standard Microsystems to implement the on-board peripheral functions of the standard version:

- An asynchronous serial port (COM1) for the console/terminal interface
- IEEE1284 bidirectional parallel port
- Floppy disk drive support
- Keyboard and mouse interface

Asynchronous Serial Port

The Super I/O controller implements two asynchronous ports (COM1 and COM2). COM1 signals are available at header J18 on the MBX board.

COM1 alone is supported on the MBX, with COM2 routed to utility connector #2 for future use. Serial interface header J18 and serial transceivers are supplied on-board for the COM1 port. No transceivers are included for COM2.

Hardware initializes the two serial ports as COM1 and COM2 with ISA I/O base addresses of $3F8 and $2F8 respectively. This default configuration also assigns COM1 and COM2 to interrupt request lines INT4 and INT3 respectively in the PCI/ISA Bridge Controller. You can change the default configuration by reprogramming the Super I/O device. For detailed programming information, refer to the PCI and ISA bus discussions in the *MBX Series Embedded Controller Programmer's Reference Guide* and to the vendor documentation for the Super I/O device.

Because entry-level versions of the MBX board are not equipped with the Super I/O controller, the MBX can derive its console/terminal interface from one of two sources:

- The COM1 port in the Super I/O device
- The SMC1 port in the MPC8*xx* processor chip itself

To select one port or the other, you set control bits in Control Register #1 (refer to the the *MBX Series Embedded Controller Programmer's Reference Guide* for details).

Parallel Port

The bidirectional parallel port found in MBX series embedded controllers may take one of two forms, depending on the board configuration determined at the time of manufacture:

- A partial IEEE1284 parallel port with both host and peripheral capability, residing in the MPC8*xx* processor itself
- A full IEEE1284 parallel port with host capability only, available in standard versions of the board (i.e., those equipped with a Peripheral I/O controller), implemented with the Super I/O device.

In either case, all parallel I/O interface signals are routed to parallel port header J13.

To select between host or peripheral mode, you set control registers in the MPC8*xx* processor (refer to the the *MBX Series Embedded Controller Programmer's Reference Guide* for details). In peripheral mode, the MPC8*xx* itself acts as a Centronics printer interface as it receives data from some other master in the system.

The signals not implemented in the partial IEEE1284 implementation are AUTOFD#, INIT, and SEL_IN. The full IEEE1284 implementation supplies those signals at the expense of the peripheral-mode capability. For detailed programming information, refer to the parallel port discussions in the *MBX Series Embedded Controller Programmer's Reference Guide* and to the vendor documentation for the Winbond Super I/O device.

2.88MB Floppy Disk Drive Controller

The Peripheral I/O controller incorporates a PS/2-compatible low- and high-density disk drive controller for use with an optional 2.88MB external disk drive. The drive interfaces with the Super I/O device via MBX board connector J17, which relays control signals.

Note Supplying power for the disk drive is up to the system integrator. Refer to Chapter 4 for the pin assignments of J17.

Hard disk drives are under the control of the EIDE interface incorporated into the Winbond PCI/ISA bridge. For a description of the EIDE interface, refer to the *PCI/ISA Bridge* section of this chapter.

Keyboard and Mouse Interface

The Standard Microsystems 37C672 I/O controller chip used to implement the on-board peripheral functions of the standard version provides ROM-based keyboard and mouse interface control. The keyboard and mouse interface signals are filtered enroute to utility connector #2.

Ethernet Interface

The MPC8*xx* processor chip used on MBX series embedded controllers incorporates an Ethernet interface that communicates with external devices by way of the SCC1 port. The SCC1 port is coupled to an Ethernet transceiver that supports both AUI and 10Base-T connections to the MBX board.

To distinguish between AUI and 10Base-T connections, it is possible either to let the ‘‘autodetect’’ capability of the transceiver come into play or to set control bits in Control Register #1

Every MBX series embedded controller is assigned an Ethernet station address. The address is $08003E*xxxxxx*, where *xxxxxx* is the unique 6-nibble number assigned to the board (i.e., every board has a different value for *xxxxxx*).

Each MBX series embedded controller displays its Ethernet station address on a label attached to the base board. In addition, the six bytes including the Ethernet station address are stored in a serial EEPROM device separate from the Ethernet transceiver. That is, the value 08003E*xxxxxx* is stored in EEPROM. The EPPCBug firmware used on MBX series boards has the capability to retrieve or set the Ethernet station address via the **CNFG** command (described in Chapter 6).

If the data in EEPROM is lost, use the number on the label attached to the board to restore it.

For the pin assignments of the AUI or 10Base-T header on the MBX, refer to Chapter 4. For detailed programming information, refer to the *MBX Series Embedded Controller Programmer's Reference Guide.*

PCMCIA Interface

A key feature of the MBX series embedded controller is the PCMCIA (Personal Computer Memory Card International Association) bus incorporated into the MPC8*xx* processor chip. PCMCIA modules offer a variety of possibilities for memory expansion and mass storage in addition to networking applications, wireless communications, and industrial I/O.

The MBX series embedded controller supports one PCMCIA Type I, II, or III slot. A 68-pin socket on the base board (XJ26) interfaces with PCMCIA Revision 2.1-compatible modules to add any desirable function.

Refer to Chapter 4 for the pin assignments of the PCMCIA connector. For detailed programming information, refer to the PCMCIA bus description in the *MBX Series Embedded Controller Programmer's Reference Guide* and to the user documentation for the PCMCIA modules you intend to use.

LCD Interface (MPC821 Only)

MBX boards equipped with an MPC821 processor chip incorporate an LCD (liquid crystal display) interface controller. The LCD controller has a built-in 256-entry color RAM. The controller supports both active and passive panels over a parallel data bus up to 9 bits wide. Output control signals are programmable for polarity and are configurable for a variety of LCD panel types.

Supplying power circuitry for the LCD panel selected is up to the system integrator. The LCD controller port routes the data to a 20-pin 2-row header (J27) on the surface of the MBX board (as illustrated in Figure 1-4).

Refer to Chapter 4 for the pin assignments of LCD connector J27. Refer to the *PowerPC™ MPC821 Portable Systems Microprocessor User's Manual* for detailed programming information.

MPC8*xx* Serial Communications Interface

The MPC8*xx* processor chip used on MBX series embedded controllers was designed with communications and portable systems applications in mind. It has a versatile communications interface with Time Slot Allocator (TSA) and Time Division Multiplexing (TDM) channels to support multiplexed as well as non-multiplexed serial I/O. The Time Slot Allocator can route any of the Serial Communication Controller channels (SCC2-SCC4) or Serial Management Controller channels (SMC1-SMC2) to the TDM channel to support communication links that require time division multiplexing.

To implement a specific communication protocol at the physical layer, it is necessary to connect the appropriate transceivers to the MBX board. The 8*xx*/COMM connector (P1), a 144-pin socket, is furnished for that purpose. All necessary TDM signals, including clocks, are routed to the 8*xx*/COMM connector so that a user-supplied add-on card with transceiver circuitry for the desired communication functions can be attached there. Signals from Serial Communication Controllers (SCCs) 2-4, Serial Management

Controllers (SMCs) 1-2, the Serial Peripheral Interface (SPI), and the Interprocessor-Integrated Controller (I^2C) are all available at the 8*xx* / COMM connector.

Note Using the MPC8*xx* processor's parallel port in an application makes the SMC2 and SPI interface signals unavailable at the 8*xx* / COMM connector. However, the remaining serial channels with TDM capability (SCC2-SCC4 and SMC1) are still present at that connector.

The TDM capability of the serial interface does not prevent you from operating the serial channels in standard non-multiplexed fashion. A mix of TDM (multiplexed) and non-multiplexed channels, or the implementation of additional EIA-232-D channels, would be equally feasible.

The pin assignments of the 8*xx* / COMM connector (821 / COMM or 860 / COMM, depending on your board configuration) are listed in Chapter 4. Note that some signal lines vary in function in accordance with the mode of operation selected. For further information on the serial communications interface, refer to the *MBX Series Embedded Controller Programmer's Reference Guide* or to the MPC821 / MPC860 processor user's manuals as applicable.

MPC8*xx* Bus Interface

In support of TDM interfaces requiring a parallel data bus or local processor bus interface, all MPC8*xx* bus interface signals (data, address, control) are routed to the 8*xx* / COMM board connector (P1), the same 144-pin socket used by the MPC8*xx* serial communications interface. In addition to servicing TDM interfaces that require bus access, routing those signals to the 8*xx* / COMM connector provides an I / O contact point for other MPC8*xx*-type devices. Those devices may, in turn, send interrupts and assume the function of bus master.

For further information on the MPC8*xx* bus interface, refer to the *MBX Series Embedded Controller Programmer's Reference Guide* or to the MPC821 / MPC860 processor user's manuals as applicable.

PC/104-*Plus* (PCI/ISA) Interface

A significant feature of the MBX series embedded controller is the PC / 104-*Plus* interface, derived from the PCI QSPAN device (see Figure 3-1). PC / 104-*Plus* modules, plug-compatible with both PCI (Peripheral Component Interconnect) and ISA (Industry Standard Architecture) buses, offer a variety of functionality as display interfaces, as network interfaces, and in industrial I / O applications.

MBX series boards comply with PCI interface specification 2.1 (although restricted to 32-bit mode) and support the P996.1 Standard for Compact Embedded PC Modules. The standard dimensions for PC / 104-*Plus* modules are 3.6 inches by 3.8 inches, but larger sizes are not precluded.

A 120-pin socket on the MBX board (P2) interfaces with PCI Revision 2.1-compatible modules to add any desirable function. A two-part 104-pin ISA socket (J21 / 22) accommodates ISA modules. PC / 104-*Plus* (PCI / ISA) modules can be intermingled with PC / 104 (ISA) modules; they can be stacked up to four high.

Refer to Chapter 4 for the pin assignments of the PC / 104 and PC / 104-*Plus* connector. For detailed programming information, refer to the PCI and ISA bus descriptions in the *MBX Series Embedded Controller Programmer's Reference Guide* and to the user documentation for the PC / 104-*Plus* modules you intend to use.

PCI/ISA Bridge Controller

The MBX series embedded controller uses a Winbond W83C553F bridge controller to supply the interface between the PCI local bus and the ISA system I / O bus (diagrammed in Figure 1-3). In addition, the PCI / ISA bridge controller provides support circuitry for standard-version boards and incorporates an EIDE interface for hard disk drives.

The PCI / ISA bridge controller provides the following functions:

- PCI bus arbitration for:
  - The PHB (Processor Host Bridge) MPU / local bus interface
  - The PC / 104-*Plus* (PCI) interface
  - The integrated PCI / EIDE interface
- ISA bus arbitration for DMA devices
- ISA interrupt mapping for four PCI interrupts
- Interrupt controller functionality to support 14 ISA interrupts
- Edge / level control for ISA interrupts
- Seven independently programmable DMA channels
- One 16-bit timer
- Three interval counters / timers

The EIDE (Enhanced Integrated Drive Electronics) interface with bus master capability supports a direct ribbon cable connection to 2 1/2-inch hard disk drives via a header (J14) on the MBX board. J14 is a standard 44-pin dual-row connector. J14 supplies +5Vdc power in addition to data and control signals, so no separate cable is needed to power the drive.

Polyswitches (Resettable Fuses)

The MBX series embedded controller draws +3.3Vdc, +5Vdc, and +12Vdc power through power connector header J12. The +5Vdc power is fused on-board at its entry to the keyboard and mouse supply circuitry. The +12Vdc power is fused on-board at its entry to the LAN circuits on the MBX. The following table lists the fuses with the voltages they protect.

Table 3-2. Fuse Assignments

Fuse	Voltage
R49	+12Vdc
R54	+5Vdc

The fuses are located on the secondary side of the board.

Connector Pin Assignments

4

MBX Series Connectors

This chapter summarizes the pin assignments for interconnect aignals on MBX series embedded controllers.

Power Connector J12

A seven-pin friction lock connector, right-angle or straight up, serves as power connector. The pin assignments for the power connector are listed in the following table.

Table 4-1. Power Connector

1	+5V
2	GND
3	GND
4	+12V
5	+3.3V
6	GND
7	+5V

Test Port Header J23

A 16-pin header (J23 on MBX series boards) provides access to an IEEE 1149 test port. The pin assignments are listed in the following table:

Table 4-2. Test Port Header

1	TDO		2
3	TDI	TRST#	4
5		+3.3V	6
7	TCK		8
9	TMS		10
11	SRESET#		12
13	HRESET#	KEY	14
15		GND	16

Debug Port Header J24

A 10-pin header (J24 on MBX series boards) provides access to debug port signals. The pin assignments are listed in the following table:

Table 4-3. Debug Port Port Header

1	VFLS0	SRESET#	2
3	GND	DSCK	4
5	GND	VFLS1	6
7	HRESET#	DSDI	8
9	+3.3V	DSDO	10

Parallel I/O Header J13

A 26-pin header (J13 on MBX series boards) provides access to the parallel I/O interface. The pinouts are arranged to permit a direct ribbon cable connection to a standard IEEE P1284-A DB25 female connector. The pin assignments are listed in the following table.

Table 4-4. Parallel I/O Header

1	STBO#	AUTOFD#	2
3	D0	FAULT#	4
5	D1	INIT#	6
7	D2	SEL_IN#	8
9	D3	GND	10
11	D4	GND	12
13	D5	GND	14
15	D6	GND	16
17	D7	GND	18
19	STB1#	GND	20
21	BUSY	GND	22
23	PERROR	GND	24
25	SEL_OUT	KEY	26

Notes AUTOFD# and SEL_IN# are not supported when the MPC8*xx* port is used. They are supported when the Super I/O controller port is used.

BUSY, PERROR, and SEL_OUT are pulled down with 4.7KΩ resistors. All other control signals are pulled up with 4.7KΩ resistors.

Serial Port Header J18

A 10-pin header (J18 on MBX series boards) provides access to the RS-232-C serial I/O interface. The pinouts are arranged to permit a direct ribbon cable connection to a DB25 male connector. The pin assignments are listed in the following table.

Table 4-5. Serial I/O Header

DB9 Pin (DTE)	Header Pin	Signal Function		Header Pin	DB9 Pin (DTE)
1	1	DCD	DSR	2	6
2	3	RXD	RTS	4	7
3	5	TXD	CTS	6	8
4	7	DTR	RI	8	9
5	9	GND		10	

Note For SMC1, only TXD and RXD are supported.

Ethernet 10Base-T Connector J15

MBX series embedded controllers provide both 10Base-T and (optionally) AUI local area network connections. The 10Base-T LAN interface is implemented with a shielded vertical-mount RJ45 socket located on the board. The pin assignments are listed in the following table.

Table 4-6. Ethernet 10Base-T Connector

1	TD+
2	TD–
3	RD+
4	No Connection
5	No Connection
6	RD–
7	No Connection
8	No Connection

Ethernet AUI Header J20

The optional AUI connection is implemented with a 16-pin header (J20) located on the MBX series board. The pin assignments are listed in the following table.

Table 4-7. Ethernet AUI Header

DB15 Pin	Header Pin	Signal Function		Header Pin	DB15 Pin
1	1	GND	CD–	2	9
2	3	CD+	TD–	4	10
3	5	TD+	GND	6	11
4	7	GND	RD–	8	12
5	9	RD+	+12V	10	13
6	11	GND	GND	12	14
7	13			14	15
8	15	GND		16	

Note If the AUI option is not present on the MBX board, header J20 and other AUI-related parts are not populated.

8*xx*/COMM Expansion Connectors

MBX series embedded controllers support EBX form factor expansion modules such as PC/104, PC/104-*Plus*, and 8XX/COMM modules. On MBX860 boards, the 860/COMM expansion connector (P1), a 144-pin high-density socket, provides the electrical connection for expansion modules. On MBX821 boards, the 821/COMM expansion connector (P1) performs a similar function. The pin assignments are listed in the following two tables.

Table 4-8. 860/COMM Expansion Connector

	Row A	Row B	Row C	Row D	
1	RETRY#	TS#	COMMINT#	CLKOUT	1
2	GND	GND	CS#	GND	2
3	TA#	BB#	Not Used	SPKROUT	3
4	GND	AS#	Not Used	HRESET#	4
5	TEA#	GND	D0	D1	5
6	GND	L1TCLKb (T4_C8)	D2	D3	6
7	SCC3TXD	B4_T4_C7	D4	D5	7
8	SCC3RXD	L1RCLKb (T3_C6)	D6	D7	8
9	SCC3RTS	B3_T3_C5	D8	D9	9
10	SCC3CTS	L1TCLKa (B2_T2_C3)	D10	D11	10
11	SCC3DCD	L1RCLKa (B1_T1_C1)	D12	D13	11
12	+5V	+3.3V	D14	D15	12
13	SCC4TXD	L1RXDa	D16	D17	13
14	SCC4RXD	L1TXDa	D18	D19	14
15	SCC4RTS	L1RXDb	D20	D21	15
16	SCC4CTS	L1TXDb	D22	D23	16
17	SCC4DCD	L1ST4	D24	D25	17
18	+12V	L1ST3	D26	D27	18
19	SMC1RXD	L1RSYNCb	D28	D29	19
20	SMC1TXD	L1TSYNCb	D30	D31	20
21	SMC1SYN	L1RSYNCa	A0	A1	21
22	+5V	L1TSYNCa	A2	A3	22
23	SMC2RXD / L1CLKOa	+3.3V	A4	A5	23
24	SMC2TXD / L1CLKOb	SCC2TXD	A6	A7	24
25	SMC2SYN	SCC2RXD	A8	A9	25
26	GND	SCC2RTS	A10	A11	26
27	SPICLK	SCC2CTS	A12	A13	27
28	SPISEL	SCC2DCD	A14	A15	28
29	SPIMISO	SIZ0	A16	A17	29
30	SPIMOSI	SIZ1	A18	A19	30
31	I2CSCL	GND	A20	A21	31
32	I2CSDA	BI#	A22	A23	31
33	BRCOMM#	DBIP#	A24	A25	31
34	BGCOMM#	BURST#	A26	A27	31
35	RD / WR#	Not Used	A28	A29	31
36	Not Used	Not Used	A30	A31	32

Table 4-9. 821/COMM Expansion Connector

	Row A	Row B	Row C	Row D	
1	RETRY#	TS#	COMMINT#	CLKOUT	1
2	GND	GND	CS#	GND	2
3	TA#	BB#	Not Used	SPKROUT	3
4	GND	AS#	Not Used	HRESET#	4
5	TEA#	GND	D0	D1	5
6	GND	L1TCLKb (T4_C8)	D2	D3	6
7	LD3	B4_T4_C7	D4	D5	7
8	LD4	L1RCLKb (T3_C6)	D6	D7	8
9	LD0	B3_T3_C5	D8	D9	9
10	L1TSYNCb	L1TCLKa (B2_T2_C3)	D10	D11	10
11	L1RSYNCb	L1RCLKa (B1_T1_C1)	D12	D13	11
12	+5V	+3.3V	D14	D15	12
13	LD1	L1RXDa	D16	D17	13
14	LD2	L1TXDa	D18	D19	14
15	LCD_AC/OE	L1RXDb	D20	D21	15
16	L1TSYNCa	L1TXDb	D22	D23	16
17	L1RSYNCa	L1ST4	D24	D25	17
18	+12V	L1ST3	D26	D27	18
19	SMC1RXD	LD5	D28	D29	19
20	SMC1TXD	LD6	D30	D31	20
21	SMC1SYN	LD7	A0	A1	21
22	+5V	LD8	A2	A3	22
23	SMC2RXD/L1CLKOa	+3.3V	A4	A5	23
24	SMC2TXD/L1CLKOb	SCC2TXD	A6	A7	24
25	SMC2SYN	SCC2RXD	A8	A9	25
26	GND	SCC2RTS	A10	A11	26
27	SPICLK	SCC2CTS	A12	A13	27
28	SPISEL	SCC2DCD	A14	A15	28
29	SPIMISO	SIZ0	A16	A17	29
30	SPIMOSI	SIZ1	A18	A19	30
31	I2CSCL	GND	A20	A21	31
32	I2CSDA	BI#	A22	A23	31
33	BRCOMM#	DBIP#	A24	A25	31
34	BGCOMM#	BURST#	A26	A27	31
35	RD/WR#	Not Used	A28	A29	31
36	Not Used	Not Used	A30	A31	32

Utility Connector J16

A 16-pin dual-row header known as ‘‘Utility Connector #1’’ supplies the interface between the MBX series embedded controller and external devices such as status LEDs, Reset and Abort switches, and power sources. The pin assignments for this utility connector are listed in the following table.

Table 4-10. Utility Connector

1	+3.3V	–12V	2
3	+5V	–5V	4
5	ResetSwitch#	Battery Plus	6
7	ETHTX LED#	Battery Minus	8
9	ETHRX LED#	Power Fail Sense#	10
11	ETHCOL LED#	Stop Interrupt#	12
13	ETHTPI LED#	GND	14
15	ETHTPP LED#	IDE LED#	16

LCD Connector J27 (MBX821)

On MBX821 models, a 20-pin dual-row header supplies the interface between the MBX821's LCD controller and the panel. The pin assignments for the LCD connector are listed in the following table.

Table 4-11. LCD Connector

1	GND	RSVD	2
3	GND	SHIFT/CLK	4
5	GND	LOAD/HSYNC	6
7	+12V	FRAME/VSYNC	8
9	+5V	LCD_AC/OE	10
11	+3.3V	LD0	12
13	LD1	LD2	14
15	LD3	LD4	16
17	LD5	LD6	18
19	LD7	LD8	20

PC/104-*Plus* (PCI) Expansion Connector P2

A 120-pin high-speed stackable socket provides an interface for PC/104-*Plus* expansion devices. The pin assignments for the PC/104-*Plus* connector are listed in the following table.

Table 4-12. PC/104-*Plus* Expansion Connector

	Row A	Row B	Row C	Row D	
1	5V Key	Reserved	+5V	AD00	1
2	VI/O	AD02	AD01	+5V	2
3	AD05	GND	AD04	AD03	3
4	C/BE0#	AD07	GND	AD06	4
5	GND	AD09	AD08	GND	5
6	AD11	VI/O	AD10	M66EN[2]	6
7	AD14	AD13	GND	AD12	7
8	+3.3V	C/BE1#	AD15	+3.3V	8
9	SERR#	GND	SB0#	PAR	9
10	GND	PERR#	+3.3V	SDONE	10
11	STOP#	+3.3V	LOCK#	GND	11
12	+3.3V	TRDY#	GND	DEVSEL#	12
13	FRAME#	GND	IRDY#	+3.3V	13
14	GND	AD16	+3.3V	C/BE2#	14
15	AD18	+3.3V	AD17	GND	15
16	AD21	AD20	GND	AD19	16
17	+3.3V	AD23	AD22	+3.3V	17
18	IDSEL0	GND	IDSEL1	IDSEL2	18
19	AD24	C/BE3#	VI/O	IDSEL3	19
20	GND	AD26	AD25	GND	20
21	AD29	+5V	AD28	AD27	21
22	+5V	AD30	GND	Ad31	22
23	REQ0#	GND	REQ1#	VI/O	23
24	GND	REQ2#	+5V	GNT0#	24
25	GNT1#	VI/O	GNT2#	GND	25
26	+5V	CLK0	GND	CLK1F	26
27	CLK2	+5V	CLK3	GND	27
28	GND	INTD#	+5V	RST#	28
29	+12V	INTA#	INTB#	INTC#	31
30	–12V	Reserved	Reserved	3.3V Key	32

Notes On the PC/104-*Plus* expansion connector, the key pins are provided to ensure that a compatible module is installed. In +5V I/O configurations, pin A1 is removed and the female side plugged. In +3.3V I/O configurations, pin D30 is similarly modified.

Signal ground (GND) corresponds to a 33MHz PCI bus ground. VI/O lines are connected to +5V.

PC/104 (ISA) Expansion Connector J21/J22

Two connectors, a 2 x 20-pin (J21) and a 2 x 32-pin (J22) socket, make up the PC/104 ISA bus expansion connector. The pin assignments for the PC/104 connector are listed in the following table.

Table 4-13. PC/104 (ISA) Expansion Connector

	Row A	Row B	Row C	Row D	
1	IOCHK#	GND	GND	GND	1
2	SD7	RSTISA	SBHE#	MEMCS16#	2
3	SD6	+5V	LA23	IOCS16#	3
4	SD5	INT9	LA22	INT10	4
5	SD4	–5V	LA21	INT11	5
6	SD3	DNT2	LA20	INT12	6
7	SD2	–12V	LA19	INT15	7
8	SD1	ENDXFR#	LA18	INT14	8
9	SD0	+12V	LA17	DACK0#	9
10	IOCHRDY	KEY	MEMR#	DRQ0	10
11	AEN	SMEMW#	MEMW#	DACK5#	11
12	SA19	SMEMR#	SD8	DRQ5	12
13	SA18	IOW#	SD9	DACK6#	13
14	SA17	IOR#	SD10	DRQ6	14
15	SA16	DACK3#	SD11	DACK7#	15
16	SA15	DRQ3	SD12	DRQ7	16
17	SA14	DACK1#	SD13	+5V	17
18	SA13	DRQ1	SD14	MASTER#	18
19	SA12	REFRESH#	SD15	GND	19
20	SA11	ISACLK	KEY	GND	20
21	SA10	INT7			
22	SA9	INT6			
23	SA8	INT5			
24	SA7	INT4			
25	SA6	INT3			
26	SA5	DACK2#			
27	SA4	TC			
28	SA3	BALE			
29	SA2	+5V			
30	SA1	OSC			
31	SA0	GND			
32	GND	GND			

EIDE Connector J14

A 44-pin dual-row header supplies a connection point for an EIDE (Enhanced IDE) hard disk subsystem. The EIDE header permits a direct ribbon cable connection between the MBX series embedded controller and user-installed 2 1/2-inch hard disk drives. The pin assignments for the EIDE connector are listed in the following table.

Table 4-14. EIDE Connector

1	RST#	GND	2
3	D7	D8	4
5	D6	D9	6
7	D5	D10	8
9	D4	D11	10
11	D3	D12	12
13	D2	D13	14
15	D1	D14	16
17	D0	D15	18
19	GND	KEY	20
21	REQA	GND	22
23	IOW#	GND	24
25	IOR#	GND	26
27	CHRDY	ALE	28
29	DACKA#	GND	30
31	IRQA	IOCS16#	32
33	A1	DIAG#	34
35	A0	A2	36
37	CS0#	CS1#	38
39	ACT#	GND	40
41	VCC	VCC	42
43	GND	RSVD	44

Floppy Disk Connector J17

A 34-pin dual-row header supplies the interface between the MBX series embedded controller and external floppy disk drives. The pin assignments for the floppy disk drive connector are listed in the following table.

Table 4-15. Floppy Disk Drive Connector

1	GND	DRVDEN0#	2
3	GND		4
5	GND	DRVDEN1#	6
7	GND	INDEX#	8
9	GND	MTR0#	10
11	GND	DRV1#	12
13	GND	DRV0#	14
15	GND	MTR1#	16
17	GND	DIR#	18
19	GND	STEP#	20
21	GND	WDATA#	22
23	GND	WGATE#	24
25	GND	TRK0#	26
27	GND	WRPR0#	28
29	GND	RDATA#	30
31	GND	HDSEL#	32
33	GND	DSKCHG#	34

Utility Connector J19

A 16-pin dual-row header known as ‘‘Utility Connector #2’’ supplies the interface between the MBX series embedded controller and external devices such as the keyboard and mouse. The pin assignments for this utility connector are listed in the following table.

Table 4-16. Utility Connector

1	KDATA	KCLK	2
3	+5V fused	MCLK	4
5	MDATA	GND	6
7	IR_TXD	GND	8
9	IR_RXD	+5V	10
11	COM2_RXD	COM2_RTS#	12
13	COM2_TXD	COM2_CTS#	14
15	Reserved	Reserved	16

EPPCBug Firmware 5

Overview

The PowerPC debugger, EPPCBug, is a versatile tool for evaluating and debugging systems built around Motorola PowerPC microcomputers. Its primary uses are to test and initialize the board hardware, determine the hardware configuration, and boot the operating system. Facilities are also available for loading and executing user programs under complete operator control for system evaluation.

The PowerPC debugger provides a high degree of functionality and user friendliness, and yet stresses portability and ease of maintenance. It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

EPPCBug includes commands for display and modification of memory, breakpoint and tracing capabilities, a powerful assembler and disassembler useful for patching programs, and a ‘‘self-test at power-up’’ feature which verifies the integrity of the main CPU board. Various EPPCBug routines that handle I/O, data conversion, and string functions are available to user programs through the System Call handler. EPPCBug consists of three parts:

- A command-driven user-interactive software debugger. It is hereafter referred to as “the debugger” or “EPPCBug.”
- A set of command-driven diagnostics, which is hereafter referred to as “the diagnostics.”
- A user interface which accepts commands from the system console terminal.

When using EPPCBug, you operate from within either the debugger directory or the diagnostic directory. The debugger prompt (`EPPC-Bug` or `EPPC-Diag`) tells you the current directory.

Because EPPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, EPPCBug executes the command and the prompt reappears. However, if you enter a command that causes execution of user target code (e.g., **GO**), then control may or may not return to EPPCBug, depending on the outcome of the user program. The flow of control in EPPCBug is described in the *PowerPC EPPCBug Firmware Package User's Manual.*

EPPCBug is similar to previous Motorola firmware debugging packages (e.g., MVME147Bug, MVME167Bug, MVME187Bug), with differences due to microprocessor architectures. These are primarily reflected in the instruction mnemonics, register displays, addressing modes of the assembler / disassembler, and the passing of arguments to the system calls.

Memory Requirements

EPPCBug requires a total of 512KB of read / write memory (i.e., DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read / write memory will place the EPPCBug memory page at locations $03F80000 to $03FFFFFF.

Implementation

EPPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, EPPCBug is contained in four socketed 32-pin PLCC Flash devices that together provide 2MB (in entry-level versions) or 4MB (in standard versions) of storage. EPPCBug itself takes up 512KB (128K words) of space; the remainder of Flash memory is available for user applications. The executable code is checksummed at every power-on or reset firmware entry, and the

result (which includes a precalculated checksum contained in the Flash devices), is verified against the expected checksum. You are cautioned against modifying the contents of Flash memory unless you take precautions to re-checksum.

Using the Debugger

EPPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `EPPC-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `EPPC-Diag` prompt appears on the screen, the debugger is ready to accept diagnotics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the Return or Enter key. This allows you to correct entry errors, if necessary, with the control characters described in the *PowerPC EPPCBug Firmware Package User's Manual.*

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PowerPC EPPCBug Firmware Package User's Manual*). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in the *PowerPC EPPCBug Firmware Package User's Manual.*

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (e.g., **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PowerPC EPPCBug Firmware Package User's Manual.*

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR / NOBR	Breakpoint Insert / Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CS	Checksum
CSAR	PCI Configuration Space READ Access

Table 5-1. Debugger Commands (Continued)

Command	Description
CSAW	PCI Configuration Space WRITE Access
DS	One Line Disassembler
DTT	Display Temperature
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
GD	Go Direct (Ignore Breakpoints)
GN	Go to Next Instruction
GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HBD	History Buffer Display
HBX	History Buffer Entry / Execution
HE	Help
I2C	I2C Device Read / Write
IOC	I / O Control for Disk
IOI	I / O Inquiry
IOP	I / O Physical (Direct Disk Access)
IOT	I / O Teach for Configuring Disk Controller
LO	Load S-Records from Host
MA / NOMA	Macro Define / Display / Delete
MAE	Macro Edit
MAL / NOMAL	Enable / Disable Macro Listing
MD, MDS	Memory Display
MM	Memory Modify
MMAP	MPC8*xx* Memory Map Display
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NIOC	Network I / O Control
NIOP	Network I / O Physical
NIOT	Network I / O Teach (Configuration)
NPING	Network Ping
OF	Offset Registers Display / Modify

Table 5-1. Debugger Commands (Continued)

Command	Description
PA / NOPA	Printer Attach / Detach
PBOOT	Bootstrap Operating System
PF / NOPF	Port Format / Detach
PFLASH	Program Flash Memory
PL	Program Load
PLH	Program Load and Halt
RD	Register Display
REMOTE	Remote
RESET	Cold / Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
SD	Switch Directories
SET	Set Time and Date
SYM / NOSYM	Symbol Table Attach / Detach
SYMS	Symbol Table Display / Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
UPM	MPC8*xx* User-Programmable Memory (UPM) Display / Read / Write
VE	Verify S-Records Against Memory
VER	Revision / Version Display
VPD	Vital Product Data (VPD) Display
WL	Write Loop

Caution

Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of Flash memory will erase everything currently contained in Flash, including the EPPCBug debugger.

VPD and ENV Commands 6

Overview

Two common tasks for which you need the factory-installed debug monitor, EPPCBug, are:

- Using the EPPCBug command **VPD** to view board-specific information that is stored in the VPD (Vital Product Data) EPROM on the MBX board.
- Using the EPPCBug command **ENV** to edit configurable EPPCBug parameters in the MBX board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

The **VPD** and **ENV** commands are both described in the *PowerPC EPPCBug Firmware Package User's Manual* (listed in the *Related Documentation* appendix). Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **VPD** and **ENV** that is specific to the debugger, along with the EPPCBug parameters that can be configured with the **ENV** command.

VPD - Display Vital Product Data

Use this command to display the board configuration data, which is resident within a serial EPROM located on the MBX board. The serial EPROM contains various elements that correspond to specific operational parameters of the board. The board structure for the MBX embedded controller is as shown in the following example:

```
Product Identifier            : MBX
Manufacturing Assembly Number  : 01-w3269F05A
Serial Number                 : 2677405
Product Configuration Options : 000000000000000
Internal Clock Speed (Hertz)  : 017D7840 (&25000000)
External Clock Speed (Hertz)  : 017D7840 (&25000000)
Reference Clock Speed (Hertz) : 00008000 (&32768)
Ethernet Address              : 08003E229470
```

The VPD EPROM is factory-configured before shipment. There is no need to modify board parameters unless the contents are corrupted.

Refer to the *Programmer's Reference Guide* (listed in the *Related Documentation* appendix) for the actual location and other information about the VPD EPROM.

Refer to the *PowerPC EPPCBug Firmware Package User's Manual* (listed in the *Related Documentation* appendix) for a description of **VPD** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all EPPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PowerPC EPPCBug Firmware Package User's Manual* for a description of the use of **ENV**. Additional information on registers in MBX series boards that affect these parameters can be found in the *Programmer's Reference Guide* for your PowerPC board.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the EPPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Access the appropriate system buses (PCI bus, local MPU bus) to determine the presence of supported controllers. (Default)

N Do not access the system buses to determine the presence of supported controllers.

```
Local SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y Reset the local SCSI bus on debugger startup.

N Do not reset the local SCSI bus on debugger startup. (Default)

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the PCI/ISA bus bridge controller. Defines the mapping of PCI interrupts to the ISA interrupt controller within the ISA bridge.

```
Firmware Command Buffer Offset = 000002C8?
```

Specifies the offset within NVRAM where firmware looks for the startup command buffer.

If EPPCBug commands are found in the startup buffer, they are executed upon system startup as though a user were entering the commands at the keyboard.

If the startup buffer begins with a null character, the firmware does not attempt to execute commands from the buffer. Instead, control of the system passes to the command line prompt.

```
Firmware Command Buffer Size = 00000200?
```

Specifies the size of the startup command buffer.

```
Firmware Command Buffer Delay = 5000?
```

Defines the number of milliseconds to wait before firmware begins executing the commands in the startup command buffer. During this delay, you may press any key to prevent the execution of the startup command buffer.

The default value produces a startup delay of five seconds.

```
Program Intermediate Load Address = 00200000?
```

Defines the address in memory where the **PL** command initially loads the program image. Once the image is loaded at the intermediate load address, its contents are evaluated and repositioned in memory as appropriate for the load image type (ELF, ROMBOOT, or binary).

```
Binary Program Load Address = 00080000?
```

Defines the address to which binary images are moved for execution. Binary images are distinct from ELF or ROMBOOT images. This parameter does not affect the load address for ELF or ROMBOOT images.

```
Binary Program Execution Offset = 00000100?
```

Defines the offset from the Binary Program Load Address that you use to establish the initial instruction pointer value for binary images. This parameter does not affect the initial instruction pointer for ELF or ROMBOOT images

```
Primary Network Controller LUN = 20?
Primary Network Device LUN = 00?
```

Jointly define the network device that is to be considered the primary network controller in the system. The networking parameters for the primary network controller are saved within the primary network controller NVRAM area.


```
Firmware Command Buffer:
['NULL' terminates entry]?
```

The firmware command buffer contains EPPCBug commands that are executed upon system startup. The commands you place in the buffer should be typed just as you would enter commands from the command line.

The string 'NULL' on a new line terminates the command line entries. In the command line buffer, you can enter all EPPCBug commands except the following:

DU	**PA**
ECHO	**TA**
LO	**VE**

Note There is no support for interactive editing of the startup command buffer. If changes to an existing set of startup commands are necessary, you will need to enter a new set of commands with changes.

Related Documentation A

Motorola Computer Group Documents

The publications listed below are referenced in this document. You can purchase manuals not shipped with this product by contacting your local Motorola sales office.

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
MBX Series Embedded Controller Installation and Use	MBXA/IH
MBX Series Embedded Controller Programmer's Reference Guide	MBXA/PG
PowerPC EPPCBug Firmware Package User's Manual	EPPCBUGA/UM
PowerPC EPPCBug Diagnostics Manual	TBD

Note Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters that represent the revision level of the document, such as "/*xx*2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "/*xx*2A1" (the first supplement to the second revision of the manual).

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

To further assist your development effort, Motorola has collected some of the non-Motorola documents in this list from the suppliers. This bundle can be ordered as part number LK-PCIKIT2.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC™ MPC821 Portable Systems Microprocessor User's Manual Literature Distribution Center for Motorola Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC821UM
PowerPC™ PowerQUICC™ MPC860 User's Manual Literature Distribution Center for Motorola Telephone: 1-800-441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC860UM
W83C553 Enhanced System I/O Controller with PCI Arbiter (PIB) Winbond Electronics Corporation Winbond Systems Laboratory 2730 Orchard Parkway San Jose, CA 95134 Telephone: (408) 943-6666 FAX: (408) 943-6668	SL82C565
Super I/O Controller Standard Microsystems Corporation 300 Kennedy Drive Hauppage, NY 11788 Telephone: 1-800-443-SEMI or (516) 435-6000 FAX: (516) 233-4260	37C672

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
QSPAN User's Manual Tundra Semiconductor Corporation 603 March Road Kanata, ON K2K 2M5, Canada Telephone: 1-800-267-7231 Telephone: (613) 592-1320 or, 695 High Glen Drive San Jose, CA 95133 Telephone: (408) 258-3600 FAX: (408) 258-3659	CA91C860-33QC

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, NY 10017-21633 Telephone: 1-800-678-4333	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, NY 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 2.0

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE P996.1 Standard for Compact Embedded PC Modules Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, NY 10017-21633 Telephone: 1-800-678-4333	IEEE P996.1
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, NY 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St. #17 Hillsboro, OR 97124 Telephone: 1-800-433-5177 or (503) 693-6232 FAX: (503) 693-8344	PCI Local Bus Specification

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: 1-800-441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com or, APDA, Apple Computer, Inc. P.O. Box 319 Buffalo, NY 14207 Telephone: 1-800-282-2732 FAX: (716) 871-6511 or, IBM 1580 Route 52, Bldg. 504 Hopewell Junction, NY 12533-6531 Telephone: (800) PowerPC or, Morgan Kaufmann Publishers, Inc. 340 Pine Street, Sixth Floor San Francisco, CA 94104-3205, USA Telephone: (415) 392-2665 FAX: (415) 982-2665	TB338/D MPRP-CHRP-01 ISBN 1-55860-394-8
PC/104 and PC/104-*Plus* Specifications PC/104 Consortium P.O. Box 4303 Mountain View, CA 94040 Telephone: (415) 903-8304 FAX: (415) 967-0995	PC/104, PC/104-*Plus*
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC or 1-800-769-3772 Telephone: (708) 296-9332	MPR-PPC-RPU-02

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA / CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, NY 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA / CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 or (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO / IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI / EIA-232-D Standard

Specifications

Table B-1 lists the general specifications for MBX series embedded controllers. Subsequent sections detail cooling requirements and FCC compliance.

A complete functional description of the MBX series embedded controllers appears in Chapter 3. Specifications for the optional expansion modules can be found in the documentation for those modules.

Table B-1. MBX Series Specifications

Characteristics	Specifications
Power requirements (Excluding keyboard, mouse)	+3.3Vdc (±5%), TBDmA typical, TBDmA maximum +5Vdc (±5%), TBDmA typical, TBDmA maximum +12Vdc (±5%), TBDmA typical, TBDmA maximum
Operating temperature	0˚C to 70˚C (32˚ to 158˚F) entry air with forced-air cooling (refer to *Cooling Requirements* section)
Storage temperature	–40˚C to +85˚ C (–40˚ to 185˚F)
Relative humidity	10% to 90% (non-condensing)
Physical dimensions (Base board only) Width Length Height	EBX form factor base board 5.75 in. (146 mm) 8.0 in. (203 mm) 0.75 in. (19 mm) w / o DIMM or PC / 104-Plus modules

B

Cooling Requirements

The Motorola MBX series family of embedded controllers is specified, designed, and tested to operate reliably with an incoming air temperature range from 0˚ to 70˚ C (32˚ to 158˚ F) with forced air cooling of the entire assembly (base board and expansion modules) at a velocity typically achievable by using a 100 CFM axial fan. Temperature qualification is performed in a Motorola development chassis. Twenty-five-watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 70˚ C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

FCC Compliance

The MBX series embedded controller was tested in an FCC-compliant chassis and meets the requirements for Class B equipment. FCC compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the FCC compliance of the equipment containing the module.

Glossary

Abbreviations, Acronyms, and Terms to Know

This glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10Base-5 An Ethernet implementation in which the physical medium is a doubly shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters. Also referred to as thicknet, or thick Ethernet.

10Base-2 An Ethernet implementation in which the physical medium is a single-shielded, 50-ohm RG58A / U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters. Also referred to as AUI, thinnet, or thin Ethernet.

10Base-T An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters. Also known as twisted-pair Ethernet.

100Base-TX An Ethernet implementation in which the physical medium is an unshielded twisted pair (UTP) of wires capable of carrying data at 100 Mbps for a maximum distance of 100 meters. Also known as fast Ethernet.

ACIA **A**synchronous **C**ommunications **I**nterface **A**dapter

AIX **A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)

architecture The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.

ASCII **A**merican **S**tandard **C**ode for **I**nformation **I**nterchange, a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8 bits to encode a total of 256 alphanumeric and control characters.

ASIC **A**pplication-**S**pecific **I**ntegrated **C**ircuit

AUI **A**ttachment **U**nit **I**nterface

BBRAM Battery Backed-up Random Access Memory

bi-endian Having big-endian and little-endian byte ordering capability.

big-endian A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

BIOS **B**asic **I**nput/**O**utput **S**ystem. The built-in program that controls the basic functions of communications between the processor and the I/O devices (peripherals). Also referred to as ROM BIOS.

BitBLT **Bit** Boundary **BL**ock **T**ransfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data need not have any particular alignment.

BLT **BL**ock **T**ransfer

board The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.

bpi **b**its **p**er **i**nch

bps **b**its **p**er **s**econd

bus The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy drives and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.

cache A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and / or instructions that the CPU is most likely to use over and over again and avoids frequent accesses to the slower hard drive or floppy disk drive.

CAS **C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.

CD **C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.

CD-ROM **C**ompact **D**isk **R**ead-**O**nly **M**emory

CFM **C**ubic **F**eet per **M**inute

CHRP See Common Hardware Reference Platform (CHRP).

CHRP-compliant See Common Hardware Reference Platform (CHRP).

CHRP Spec See Common Hardware Reference Platform (CHRP).

CISC **C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.

CODEC **CO**der / **DEC**oder

Color Difference (CD) The signals of (R-Y) and (B-Y) without the luminance (-Y) signal. The Green signals (G-Y) can be extracted by these two signals.

Common Hardware Reference Platform (CHRP)
A specification published by the Apple, IBM, and Motorola which defines the devices, interfaces, and data formats that make up a CHRP-compliant system using a PowerPC processor.

Composite Video Signal (CVS/CVBS)
Signal that carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as “Baseband Video”.

cpi	**c**haracters **p**er **i**nch
cpl	**c**haracters **p**er **l**ine
CPU	**C**entral **P**rocessing **U**nit. The master computer unit in a system.
DCE	**D**ata **C**ircuit-terminating **E**quipment.
DLL	**D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.
DMA	**D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.
DOS	**D**isk **O**perating **S**ystem
dpi	**d**ots **p**er **i**nch
DRAM	**D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extremely high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.
DTE	**D**ata **T**erminal **E**quipment.
ECC	**E**rror **C**orrection **C**ode
ECP	**E**xtended **C**apability **P**ort
EEPROM	**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.
EIDE	**E**nhanced **I**ntegrated **D**rive **E**lectronics. An improved version of **IDE**, with faster data rates, 32-bit transactions, and DMA. Also known as **Fast ATA-2**.
EISA (bus)	**E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of the 16-bit or 8-bit units that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.
EPP	**E**nhanced **P**arallel **P**ort

EPROM — **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.

ESCC — **E**nhanced **S**erial **C**ommunication **C**ontroller

ESD — **E**lectro-**S**tatic **D**ischarge / Damage

Ethernet — A local area network standard that uses radio frequency signals carried by coaxial cables.

fast Ethernet — See 100Base-TX.

FDC — **F**loppy **D**isk **C**ontroller

FDDI — **F**iber **D**istributed **D**ata **I**nterface. A network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at speeds up to 100 Mbps.

FIFO — **F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

firmware — The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).

frame — One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.

graphics controller — On EGA and VGA, a section of circuitry that can provide hardware assistance for graphics-drawing algorithms by performing logical functions on data written to display memory.

HAL — **H**ardware **A**bstraction **L**ayer. The lower-level hardware interface module of the Windows NT operating system. It contains platform-specific functionality.

hardware The term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system. A computing system is normally spoken of as having two major components: hardware and software.

HCT **H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.

I/O **I**nput/**O**utput

IBC PCI/**I**SA **B**ridge **C**ontroller

IDC **I**nsulation **D**isplacement **C**onnector

IDE **I**ntegrated **D**rive **E**lectronics. A disk drive interface standard. Also known as **ATA** (**A**dvanced **T**echnology **A**ttachment).

IEEE **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers

interlaced A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. Its advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware and may also make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.

IQ Signals Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

ISA (bus) **I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)

ISASIO **ISA S**uper **I**nput/**O**utput device

ISDN	**I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.
LAN	**L**ocal **A**rea **N**etwork
LED	**L**ight-**E**mitting **D**iode
LFM	**L**inear **F**eet per **M**inute
little-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.
MBLT	**M**ultiplexed **BL**ock **T**ransfer
MCA (bus)	**M**icro **C**hannel **A**rchitecture
MCG	**M**otorola **C**omputer **G**roup
MFM	**M**odified **F**requency **M**odulation
MIDI	**M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.
MPC	**M**ultimedia **P**ersonal **C**omputer
MPIC	**M**ulti-**P**rocessor **I**nterrupt **C**ontroller
MPU	**M**icro**P**rocessing **U**nit
MTBF	**M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power-on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how long a device or any individual component is likely to last, nor is it a warranty, but rather an indicator of the relative reliability of a family of products.
multisession	The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.

non-interlaced A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

nonvolatile memory A memory in which the data content is maintained whether the power supply is connected or not.

NTSC **N**ational **T**elevision **S**tandards **C**ommittee (USA)

NVRAM **N**on-**V**olatile **R**andom **A**ccess **M**emory

OEM **O**riginal **E**quipment **M**anufacturer

OMPAC **O**ver-**M**olded **P**ad **A**rray **C**arrier

OS **O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.

OTP **O**ne-**T**ime **P**rogrammable

palette The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144.

parallel port A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.

PCI (local bus) **P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.

PCMCIA (bus) **P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.

PCR **P**CI **C**onfiguration **R**egister

PHB **P**CI **H**ost **B**ridge

PDS **P**rocessor **D**irect **S**lot

physical address A binary address that refers to the actual location of information stored in secondary storage.

PIB — **P**CI-to-**I**SA **B**ridge

pixel — An acronym for picture element, also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

PLL — **P**hase-**L**ocked **L**oop

PMC — **P**CI **M**ezzanine **C**ard

POWER — **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)

PowerPC™ — The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 601™ — The first implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 256-entry buffer and a 32KB unified (instruction and data) cache. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 601 is used by Motorola, Inc. under license from IBM.

PowerPC 603™ — The second implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and an 8KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 603 is used by Motorola, Inc. under license from IBM.

PowerPC 604™ — The third implementation of the PowerPC family of microprocessors currently under development. PowerPC 604 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP)
A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PowerStack™ RISC PC (System Board)
A PowerPC-based computer board platform developed by the Motorola Computer Group. It supports Microsoft's Windows NT and IBM's AIX operating systems.

PRP See PowerPC Reference Platform (PRP).

PRP-compliant See PowerPC Reference Platform (PRP).

PRP Spec See PowerPC Reference Platform (PRP).

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem / **2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Reduced-Instruction-Set Computer (RISC)
A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced-Instruction-Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC **R**eal-**T**ime **C**lock

SBC	**S**ingle **B**oard **C**omputer
SCSI	**S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. The SCSI-1 implementation provides up to 5 Mbps data transfer.
SCSI-2 (Fast/Wide)	An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.
serial port	A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.
SIM	**S**erial **I**nterface **M**odule
SIMM	**S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) that is designed to fit into a standard slot.
SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Instead, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	The term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. A computing system is normally spoken of as having two major components: hardware and software. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer

standard(s) A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.

SVGA **S**uper **V**ideo **G**raphics **A**rray (IBM). An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 800 x 600 pixels.

Teletext One-way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.

thick Ethernet See 10Base-5.

thin Ethernet See 10Base-2.

twisted-pair Ethernet See 10Base-T.

UART **U**niversal **A**synchronous **R**eceiver/**T**ransmitter

UV **U**ltra**V**iolet

UVGA **U**ltra **V**ideo **G**raphics **A**rray. An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Vertical Blanking Interval (VBI) The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is on the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

VESA (bus) **V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.

VGA **V**ideo **G**raphics **A**rray (IBM). The third and most common monitor standard used today. It provides up to 256 simultaneous colors and a screen resolution of 640 x 480 pixels.

virtual address A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.

VL bus See **V**ESA **L**ocal bus (VL bus).

volatile memory A memory in which the data content is lost when the power supply is disconnected.

VRAM **V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

XGA E**X**tended **G**raphics **A**rray. An improved IBM VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Y Signal Luminance. Parameter that determines the brightness (but not the color) of each spot (pixel) on a CRT screen in color or B/W systems.

Index

INDEX