

# **Micro Computer Control Corporation**

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# I<sup>2</sup>C Bus Technical Overview



The I<sup>2</sup>C (Inter-Integrated Circuit) Bus is a two-wire, low to medium speed, communication bus (a path for electronic signals) developed by Philips Semiconductors in the early 1980s. I<sup>2</sup>C was created to reduce the manufacturing costs of electronic products. It provides a low-cost, but powerful, chip-to-chip communication link within these products. Initial applications for I<sup>2</sup>C included volume and contrast control in radios and televisions. Over the past decade, I<sup>2</sup>C

has expanded its communications role to include a wide range of applications.

Today, I<sup>2</sup>C can be found in a wide variety of computer, industrial, entertainment, medical, and military systems, with almost unlimited growth potential.

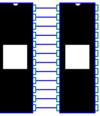
# Industry Standard

The "I<sup>2</sup>C Bus Specification," published by Philips Semiconductor, provides a communication protocol definition of the signal activity on the I<sup>2</sup>C Bus. This specification helps instruct semiconductor device manufacturers, and electronic product developers, in the correct use of the technology. The specification is freely available on the Internet (www.semiconductors.philips.com/buses/i2c/).

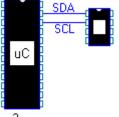
#### Low Cost

Prior to  $I^2C$ , chip-to-chip communications used many wires in a parallel interface, often requiring ICs (integrated circuits) to have 24, 28, or more pins. Many of these pins were used for inter-chip addressing, selection, control, and data transfers. In a parallel interface, 8 data bits are typically transferred from a sender IC to a receiver IC in a single operation.

 $I^2C$  performs chip-to-chip communications using only two wires in a serial interface, allowing ICs to communicate with fewer pins. The two wires in the  $I^2C$  Bus are called Clock (SCL) and Data (SDA). These two wires carry addressing, selection, control, and data, one bit at a time. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the transfer. ICs that use the  $I^2C$  Bus can perform the same function as their larger parallel interface counterparts, but with far fewer pins. This greatly reduces the size and cost of ICs based on the  $I^2C$  Bus.



Parallel Interface

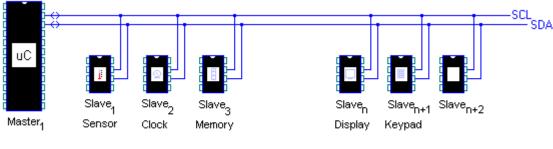


I<sup>2</sup>C Serial Interface

A second savings from the two-wire  $I^2C$  Bus design is in printed circuit board (PCB) size and costs. With ICs based on the  $I^2C$  Bus needing far fewer wires (copper traces) for inter-chip communications, circuit boards using  $I^2C$  ICs are greatly reduced in size, complexity, and cost.

# More Power

Although cost savings alone would be enough to make the I<sup>2</sup>C Bus a success, its developers were also charged with creating a powerful communication link. I<sup>2</sup>C meets this challenge by supporting several powerful features.



One I<sup>2</sup>C Master, Multiple Slaves

# Master-Slave Hierarchy

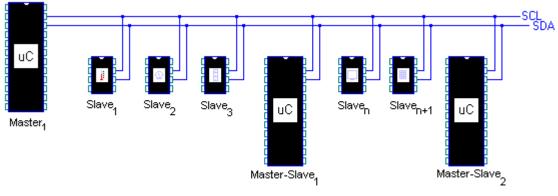
I<sup>2</sup>C devices are classified as master or slave. A device that initiates a message is called a master, while a device that responds to a message is called a slave. A device can be master-only, slave-only, or switch between master and slave, as the application requires.

# Multiple Devices

 $I^2C$  can connect many ICs on just two-wires. Each  $I^2C$  slave device has its own unique slave address. When a master sends a message, it includes the slave address at the beginning of the message. All devices on the bus hear the message, but only the slave that recognizes its own address participates in the transfer.

#### Multi-Master Support

I<sup>2</sup>C also supports multiple master devices on the bus at the same time, a powerful feature that optimizes bus use by keeping bus message traffic to a minimum. To support multiple masters, I<sup>2</sup>C must resolve signal conflicts, should two or more master devices try to talk on the bus at the same time. This feat, called bus arbitration loss detection, allows a master to detect when its bus signals are conflicting with those of another master. A master that detects arbitration loss terminates its use of the bus, allowing the message generated by another master to cross the bus unharmed.



Multi-Master, Multi-Slave

#### Summary

The I<sup>2</sup>C Bus is a time-proven, industry standard, communication protocol used in a wide variety of electronic products. I<sup>2</sup>C is found in products we use every day, like cellular and conventional telephones, computers, and ATMs (automatic teller machines). Its low cost and powerful features make I<sup>2</sup>C ideal for low to medium speed chip-to-chip communications.

I<sup>2</sup>C is supported by a large and growing number of semiconductor and system manufacturers. These companies offer a variety of electronic devices, including memories, input and output devices, sensors of many types, real-time clocks, displays, data entry devices, and much more. I<sup>2</sup>C is an effective technology that can lower product costs and increase product performance.

For more information about the I<sup>2</sup>C Bus, applications, tools, and components, visit MCC's website at www.mcc-us.com.

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